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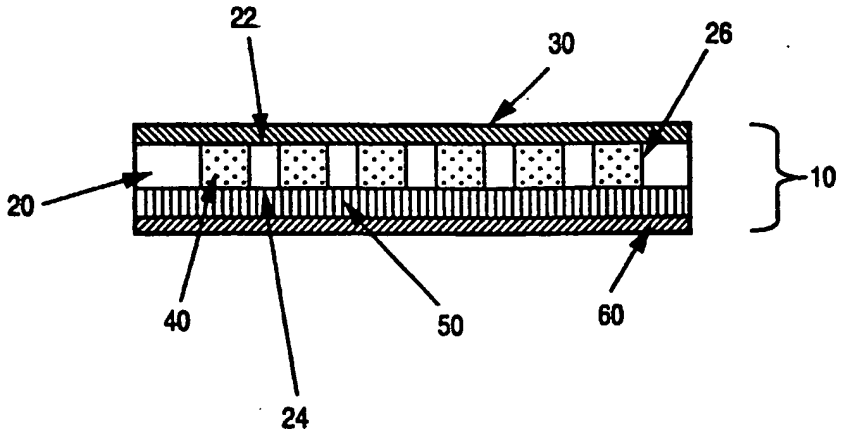
(54) Title: IRREVERSIBLE HUMIDITY INDICATOR CARDS



(57) Abstract: An irreversible humidity indicator card comprising an intermediate carrier member containing one or more holes, a clear, water vapor permeable first outer layer secured to the first side of the carrier member, a deliquescent material contained within the holes in the carrier member, a dark colored, absorbent sheet material secured to the back side of the carrier member to cover the holes in the carrier member and a second outer layer which covers the colored absorbent sheet material and a portion or all of the back side of the intermediate carrier member.

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(54) Inhibitor parcel and method for preserving electronic devices or electronic parts.

(57) Disclosed are an inhibitor parcel comprising (a) a composition comprising an unsaturated fatty acid compound as its main ingredient and (b) a permeable diffusing-parcelling material prepared by laminating and bonding an oxygen-permeable resin layer onto one side of a base sheet made of a fibrous material and an adhesive or onto one adhesive-coating side of a base sheet made of a fibrous material, then laminating and bonding thereonto an oxygen-permeable resin layer and laminating and bonding a porous film of low softening point resin or a low softening point unwoven fabric onto the other side of the base sheet, said permeable diffusing-parcelling material (b) having an oxygen permeability of 10^4 to 10^5 ml/m^2•Atm•Day and a (water vapor permeability/oxygen permeability) ratio of 0.02 [H_2O mg•Atm/O_2 ml] or above at 25° C at a relative humidity of 50% and said composition (a) being parcelled by said permeable diffusing-parcelling material (b) and an inhibitor parcel for use in electronic devices and electronic parts which comprises said inhibitor parcel and a method for preserving electronic devices and electronic parts using said inhibitor parcel.

EP 0 424 855 A1

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00889084 **Image available**
IRREVERSIBLE HUMIDITY INDICATOR **CARDS**
CARTES INDIQUANT L'HUMIDITE DE MANIERE IRREVERSIBLE
Patent Applicant/Assignee:
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Inventor(s):
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Patent and Priority Information (Country, Number, Date):
Patent: WO 200223183 A2-A3 **20020321** (WO 0223183)
Application: WO 2001US28002 20010907 (PCT/WO US0128002)
Priority Application: US 2000660560 20000912
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Main International Patent Class: G01N-031/22
Publication Language: English
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Detailed Description
Claims
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English Abstract
An irreversible **humidity indicator** card comprising an intermediate carrier member containing one or more holes, a clear, water vapor permeable first outer layer secured to the first side of the carrier member, a deliquescent material contained within the holes in the carrier member, a dark colored, absorbent sheet material secured to the back side of the carrier member to cover the holes in the carrier member and a second outer layer which covers the colored absorbent sheet material and a portion or all of the back side of the intermediate carrier member.

French Abstract
Une carte indiquant l'humidite de maniere irreversible comprend un element formant support intermediaire comprenant un ou plusieurs trous, une premiere couche externe transparente permeable a la vapeur d'eau fixee sur le premier cote de l'element formant support, un materiau deliquescent loge dans les trous de l'element formant support, un materiau en feuille, absorbant, de couleur sombre fixe sur le cote arriere de l'element formant support destine a recouvrir les trous formes dans l'element formant support et une deuxieme couche externe qui recouvre le materiau en feuille, absorbant, colore et une partie ou la totalite du cote arriere de l'element formant support intermediaire.

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Publication 20020321 A2 Without international search report and to be republished upon receipt of that report.
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Republication 20020627 A3 With international search report.
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IRREVERSIBLE HUMIDITY INDICATOR **CARDS**
Patent and Priority Information (Country, Number, Date):
Patent: ... **20020321**
Fulltext Availability:
Detailed Description
Claims

English Abstract
An irreversible **humidity indicator** card comprising an intermediate carrier member containing one or more holes, a clear, water vapor...
Publication Year: **2002**

Detailed Description
Title
IRREVERSIBLE **HUMIDITY INDICATOR** CARDS
Background of the Invention
1. Field of the Invention
This invention relates to. **humidity indicator** cards and more particularly, to an irreversible **humidity indicator** card, which is covered on both sides, which utilizes a deliquescent material which does not...

...To address the need for the detection of humidity levels within shipping or storage containers, humidity **indicators** have been developed. There are generally two types of **humidity indicators** . One of."these **humidity indicators** reversibly changes color upon exposure to particular humidity levels. Such reversible **humidity indicators** typically utilize **cobalt chloride** as the **humidity indicator** material. It changes color when exposed to predetermined levels of humidity and returns to its original color when the humidity level drops below that predetermined level. These reversible **humidity indicators** are used to indicate the current condition of a **desiccant** and/or the current humidity level within the storage container.

The second type of **humidity indicator** is an irreversible **humidity indicator** . These indicators are designed to detect a predetermined level of humidity and provide a visual indication of whether components stored in the containers where these **humidity indicators** are used have been exposed to that predetermined level of humidity even for short periods...

...falls dramatically depending upon the temperature of the surrounding air. Under these conditions, a reversible **humidity indicator** might fail to indicate the temporary presence of high humidity within a storage container even...

...cause damage to the components present in the storage container.

One of the first irreversible **humidity indicator**
2
devices was disclosed in U. S. Patent No. 2, 214, 354, which disclosed the...

...maintain a consistently low humidity level, shipping containers and long term storage containers usually contain

desiccant materials. These **desiccant** materials dehydrate the storage area and are intended to maintain the humidity level within that...

...area at a predetermined level.

These containers are periodically opened to recharge or replace the **desiccant** materials placed within the container and/or to check the level of humidity in the storage container. After replacing the **desiccant** material, the container is again sealed. In order to determine whether the humidity level in these storage containers has ever reached certain critical levels, irreversible **humidity indicators** are also often placed within the containers with 3
the **desiccant** materials. These irreversible **humidity indicators** can be reviewed at the same time that the **desiccant** material is being checked to determine whether a harmful humidity level has ever been reached in the shipping container.

A series of relative **humidity indicators** , each utilizing a different deliquescent salt, are disclosed in a series of patents which were...

...2f460f070r 2f460r071r
2r460f072r 2f460r073r 2F460r074r 2r526,938r 2f580,737f and 2f627,505. In addition, some **humidity indicator** cards are capable of showing different levels of humidity on the same card by use...

...color at varying humidity levels, as disclosed in U.S. Patent No. 2,249,867.

Humidity indicator sheets and cards which contain deliquescent salts and dyes have commonly been used to detect...
...U.S. Patent Nos. 2,249,867,
4r034f609r 4fl50,570, and 4,854fl60. Button-type **humidity , indicators** or 'plug" **humidity indicators** are also sometimes used with packaging material and are disclosed, for example, by U.S...

...containing a reflective layerf which is useful in viewing the changes in color of a **humidity indicator** card is disclosed by U.S. Patent No. 4f034r609.

A reversible **humidity indicator** card contained within tran'sparentf flexible sheet materials with an impermeable front layer is disclosed in U.S. Patent No. 5,224,373. This **humidity indicator** card is specifically designed for utilization with **electronic components** . It is formed as a NN window' in a barrier **bag** .

A delayed action, irreversible **humidity indicator** card is disclosed in U.S. Patent No. 4f793fl80.

All irreversible **humidity indicator** cards known hitherto are based on combinations of deliquescent salts and water-soluble dyes. In order to prepare **humidity indicator**

cards that react at various humidity levels, different combinations of deliquescent salts and dyes must...to determine whether a particular humidity level has been reached. W.B. Abel: Chemical Maximum **Humidity Indicator** Update Report, BDX 1989 and U.S. 3,r898r172 teach that only certain combinations of...

...salts with the dye is an additional required step for the production of the irreversible **humidity indicators** previously known. If the chosen salt and dye have different particle sizes, inhomogeneous distribution of...

...may occur and lead to inhomogeneous color and appearance on the indicating spot of the **humidity indicator** . This problem can be overcome by milling salt and dye together, but this is not...

...melt can cause corrosion to the products stored in the shipping containers in which the **humidity indicator** cards are utilized.

In addition, the blotter paper used to form 6 conventional **humidity indicator** cards sometimes sheds paper fibers and lint. Such fibers and lint may damage products that...

...as electronic components.

Accordingly, it is an object of this invention to produce an irreversible **humidity indicator** card which solves the problems present with conventional irreversible **humidity indicator** cards.

It is a still further object of the invention to disclose an irreversible **humidity indicator** card which is formed of a composite structure which includes a darkened blotter paper which...

...level of humidity.
It is a further object of the invention to disclose an irreversible **humidity indicator** card which does not use a dye with its deliquescent material.

It is a further object of the invention to disclose an irreversible **humidity indicator** card which does not produce paper fibers or lint when in use.

Summary of the Invention
This invention is directed to an irreversible **humidity indicator** card comprising an intermediate carrier member, containing front and back sides and one or more...

...permeable first outer material and/or the second outer layer further comprise materials with anti- **static** and/or **electrostatic** charge dissipative properties.

The invention is also directed to a process for the production of the above-referenced irreversible **humidity indicator** card comprising
preparing an intermediate carrier member containing a front and back side and one...

...member.

Brief Description of the Drawings
Figure 1 is a side view of the irreversible **humidity indicator** card of the invention.

Figure 2 is a perspective, exploded front view of the irreversible **humidity indicator** card.

Figure 3 is a back view of the irreversible **humidity indicator** card without the second outer layer (60).

Description of a Preferred Embodiment
Referring to Figures 1, 2 and 3, the invention is an
9
irreversible **humidity indicator** card (10) comprised of an intermediate carrier member (20), a first outer layer (30), deliquescent...

...member
(20).

The intermediate carrier member is preferably formed from a single sheet of a **moisture absorbent** material, such as a conventional blotter paper. One or more ...and placement of the holes (26) dependent on the need
of the manufacturer of the **humidity indicator** cards (10).

10
Written information informing the user of the **humidity indicator** card (10) about the humidity levels determined by the **humidity indicator** card (10) is generally printed on the front side (22) of the intermediate carrier member...

...humidity level of
the surrounding air within the time predetermined by the manufacturer of the **humidity indicator** card (10) . One preferred first outer layer (30) is a thin cellophane material. Alternatively, a...

...The choice as to the particular
deliquescent material (40) depends on the manufacturer of the **humidity indicator** card (10). A list of deliquescent salts that may be useful can be found in W.B. Abel.

"Chemical Maximum **Humidity Indicator** Update Report". BDX613-1989 and includes ZnC'21 ZnBr., ZnI . LiCl. LiBr,, LiI.

KC2H3021 CaC...thin flexible PVC material is used.

In an alternative embodiment, the composition of the irreversible **humidity indicator** (10) also preferably includes a material which introduces **electrostatic** charge dissipating and/or anti- **static** properties to the

irreversible **humidity indicator** (10). The material which introduces **electrostatic** dissipating and/or anti- **static**
16
properties may be incorporated into the clear water vapor permeable first outer layer (30) and/or into the second outer layer (60). The material which introduces **electrostatic** charge dissipating and/or anti- **static** properties is preferably selected from the group consisting of carbon products, anionic surfactants, cationic surfactants...

...30) and/or the second outer layer (60) may consist of plastic material that is **electrostatic** charge dissipative by nature, such as cellulose derivatives.

In the process of formation of the irreversible **humidity indicator** card (10). the intermediate carrier member (20), which is preferably a conventional blotting paper, is...

...outer layer (30).

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In use, this card (20) can be placed in a shipping **container** or storage **container** for equipment, preferably electronic equipment or **electronic components** , such as **integrated circuits** . Humidity present in the air within the **container** passes through at least the clear,, water vapor permeable, first outer layer (30) to be...

...intermediate carrier member (20) only after the deliquescent material (50) liquifies. Once liquification occurs, the **humidity indicator** card (10) shows that the predetermined

Claim
1 An irreversible **humidity indicator** card, comprising
an intermediate carrier member, containing one or more holes passing through the intermediate...

...of
the intermediate carrier member, which covers the colored, absorbent sheet material.

2 The irreversible **humidity indicator** card of Claim I wherein the water vapor permeable first outer layer further comprises a material exhibiting **electrostatic** charge dissipating or anti- **static** properties.

3 The irreversible **humidity indicator** card of Claim wherein the second outer layer further comprises a material exhibiting **electrostatic** charge dissipating or anti- **static** properties.
4 The irreversible **humidity indicator** card of Claim
21
, wherein the water vapor permeable, first outer layer is coated on one side with an adhesive material.

5 The irreversible **humidity indicator** card of Claim

I wherein the second outer layer is comprised of a water vapor permeable material.

6 The irreversible **humidity indicator** card of Claim 1 wherein the second outer layer is coated with an adhesive material.

7 The irreversible **humidity** indicator of Claim 1 wherein the second outer layer completely covers the back side of the intermediate carrier member.

8 The irreversible **humidity indicator** card of Claim 1 wherein the deliquescent material is selected from the group consisting of...

...two or more deliquescent salts with one or more non-ionic compounds.

9 The irreversible **humidity indicator** card of Claim 1 wherein the deliquescent material is white in color.

10 The irreversible **humidity indicator** card of Claim 1 further comprising a plurality of deliquescent materials, 22
each of which liquifies at a different, predetermined humidity level.

11 The irreversible **humidity indicator** card of Claim 1 wherein the deliquescent material does not include a dye material.

12 The irreversible **humidity indicator** card of Claim 1 wherein the clear, water vapor permeable first outer layer has a vapor transmission rate of at least about jg/ (M2 -day).

13 The irreversible **humidity indicator** card of Claim 1 wherein the colored, absorbent sheet material is produced from a colored blotting sheet.

14 The irreversible **humidity indicator** card of Claim 1 wherein the second outer layer covers the back side of the intermediate carrier member.

15 The irreversible **humidity indicator** card of Claim 1 wherein the second outer layer is secured at one or more...

...the clear,, water vapor permeable, first outer layer.

16 A process of manufacture of a **humidity indicator** card comprising
preparing an intermediate carrier member containing one or more holes, a front side...

...intermediate carrier member with a second outer layer.

17 A process of manufacture of a **humidity indicator** card comprising
preparing an intermediate carrier member containing one or more holes and a front...

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(72) Inventors: **DICK, Stefan**; 8204 William Moyers Ave., NE, Albuquerque, NW 87122 (US). **ROBERTSON, Andrew, J.**; 900 Laguayra NE, Albuquerque, NM 87108 (US).

MARTIN, Michelle, B.; 2450 Verna Court, Palm Springs, CA 92262 (US).

(74) Agent: **COX, Scott, R.**; Lynch, Cox, Gilman & Mahan, P.S.C., 400 West Market Street, Suite 2200, Louisville, KY 40202 (US).

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

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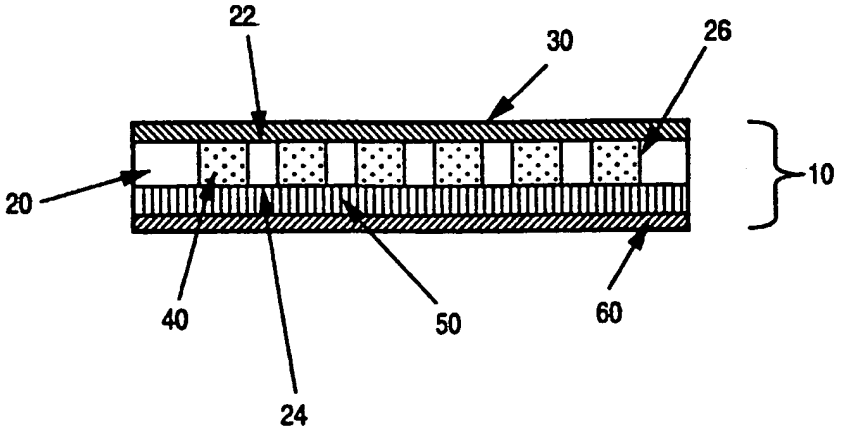
(54) Title: IRREVERSIBLE HUMIDITY INDICATOR CARDS



(57) Abstract: An irreversible humidity indicator card comprising an intermediate carrier member containing one or more holes, a clear, water vapor permeable first outer layer secured to the first side of the carrier member, a deliquescent material contained within the holes in the carrier member, a dark colored, absorbent sheet material secured to the back side of the carrier member to cover the holes in the carrier member and a second outer layer which covers the colored absorbent sheet material and a portion or all of the back side of the intermediate carrier member.

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00848420 **Image available**
AUTOMATED MANUFACTURING CONTROL SYSTEM
SYSTEME AUTOMATISE DE CONTROLE DE FABRICATION
Patent Applicant/Assignee:
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Patent Applicant/Inventor:
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DUBOIS Vincent, 15 chemin du Versant Ouest, Canton de Shefford, Quebec J0E 2N0, CA, CA (Residence), CA (Nationality), (Designated only for: US)
Legal Representative:
SOFIA Michel (et al) (agent), Swabey Ogilvy Renault, 1981 McGill College Avenue, Suite 1600, Montreal, Quebec H3A 2Y3, CA,
Patent and Priority Information (Country, Number, Date):
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Application: WO 2001CA559 20010420 (PCT/WO CA0100559)
Priority Application: CA 2306304 20000420; CA 2321009 20000927; CA 2326301 20001117; CA 2326218 20001117
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(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G05B-019/418
Publication Language: English
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Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 13208

English Abstract
An automated manufacturing control system is proposed to greatly reduce the human interaction relative to the data transfer, physical verification and process control associated with the movement of components, tooling and operators in a manufacturing system. This is achieved by the use of data carriers which are attached to the object(s) to be traced. These data carriers (12) can store all the relevant identification, material and production data required by the various elements, e.g. stations, of the manufacturing system. Various readers, integrated with controllers and application software, are located at strategic points of the production area, including production machines and storage areas, to enable automatic data transfer and physical verification that the right material is at the right place at the right time, using the right tooling.

French Abstract
L'invention concerne un systeme automatise de controle de fabrication permettant de reduire dans une large mesure l'interaction humaine relative aux transferts de donnees, aux verifications physiques et aux

controles de processus associes au deplacement des composants, a l'outillage et aux operateurs dans un systeme de fabrication. Ce resultat est obtenu en utilisant des supports de donnees qui sont lies aux objets dont on veut suivre la localisation. Ces supports de donnees (12) peuvent memoriser toutes les donnees appropriees d'identification, de materiau et de production requises par les divers elements, par exemple, postes de travail, du systeme de fabrication. Divers lecteurs, integres aux unites de controle et aux logiciels d'application sont localises a des points strategiques de la zone de production, y compris les machines de production et les aires d'entreposage pour permettre les transferts de donnees et les verifications physiques automatiques, de facon que le materiau approprie soit a sa vraie place au moment voulu tout en utilisant l'outillage approprie.

Legal Status (Type, Date, Text)

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Search Rpt	20020822	Late publication of international search report
Republication	20020822	A3 With international search report.
Search Rpt	20020822	Late publication of international search report
Correction	20021024	Corrected version of Pamphlet: pages 1-28, description, replaced by new pages 1-28; pages 29-38, claims, replaced by new pages 29-38; pages 1/9-9/9, drawings, replaced by new pages 1/9-9/9; due to late transmittal by the receiving Office
Republication	20021024	A3 With international search report.

Patent and Priority Information (Country, Number, Date):
  Patent: ... **20011101**
Fulltext Availability:
  Detailed Description
  Claims
Publication Year: **2001**

Detailed Description

... clip in accordance with a first embodiment of the present invention, shown mounted on an **electronic components** ' **tray** (that is offly partly illustrated) Fig. 3b is an enlarged elevational view of part of...reliable and convenient method of cominunic.ation with the tags (transponders). It is customised for **plastic trays** and reels and the associated tags. The support 14 is a **plastic** enclosure that is ergonomically shaped to hold **trays** and, reels 16 and at the same time to support and protect the inain antenna...rear view thereof The clip 30 is made out of process compatible materials that are **ESD** (**electrostatic** discharge) sensitive,
that can sustain at least 125 'C and that will not contaminate parts...42 that will acconunodate the transponder 12 temporarily. This pouch 42 is made out of **ESD** sensitive material, designed and sized to accept the transponder 12 easily, hold (inverted exclamation mark...
...transponder 12
to a flat surface.

Example of data structure : trans@ onder attached to a **tray** , such as **tray** 28 in
p
Fig. 3a, with **electronic components** .

Tray Identification
Manufacturer
Part number
Revision or Engineering change number
Date code
Component Identification
Manufacturer
15...This was not previously possible due to the absence of material identification on a standard **plastic** **tray** . This information can also be listed on a computer display. This list Moisture sensitive components ...

...trays or reels, must be placed by the manufacturer inside of sealed dry bags with **desiccants** and **humidity** **indicators** . The bag seal date must be indicated on the label (Fig. 1).

Once these bags...

Claim
... as claimed in claim 3, wherein said at least one component is a moistare sensitive **electronic** **component** nonnally stored in a sealed **container** adapted to be opened at at least one predetennined stage of said plurality of stages...

28/5,K/11 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00844469 **Image available**
DESICCANT **CONTAINING PRODUCT CARRIER**
SUPPORTS DE PRODUITS RENFERMANT UN DESSICCATIF
Patent Applicant/Assignee:
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Patent and Priority Information (Country, Number, Date):
Patent: WO 200178113 A1 **20011018** (WO 0178113)
Application: WO 2000US30730 20001108 (PCT/WO US0030730)
Priority Application: US 2000543346 20000405
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(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
Main International Patent Class: H01L-021/00
Publication Language: English
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Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 2380

English Abstract
Disclosed is a product carrier having a **desiccant** incorporated therein and a method for making the same. The inventive carrier reduces the number of steps required to package a semiconductor device.

French Abstract
L'invention concerne un support de produit incorporant un dessiccatif ainsi qu'un procede de preparation relatif. Ce support permet de reduire le nombre d'etapes necessaires a l'emballage d'un dispositif semi-conducteur.

Legal Status (Type, Date, Text)
Publication 20011018 A1 With international search report.
Examination 20020110 Request for preliminary examination prior to end of 19th month from priority date

DESICCANT **CONTAINING PRODUCT CARRIER**
Patent and Priority Information (Country, Number, Date):
Patent: ... **20011018**
Fulltext Availability:
Detailed Description
Claims

English Abstract
Disclosed is a product carrier having a **desiccant** incorporated therein and a method for making the same. The inventive carrier reduces the number...
Publication Year: **2001**

Detailed Description
DESICCANT CONTAINING PRODUCT CARRIER

TECHNICAL FIELD
The present invention relates to a product carrier that has a **desiccant** incorporated therein.

The present invention is particularly applicable in reducing the steps required to package...

...of product quality from the factory floor to the customer 1 0 are required.

Some **IC packages** are susceptible to moisture induced damage. The risk of this is highest when plastic encapsulation materials are used, as **plastic** is naturally permeable to moisture. The moisture in the **package** will increase or decrease to reach the Relative Humidity (RH) of the surrounding environment.

1...
...circuits includes baking the integrated circuit devices until dry, placing them into a water and **humidity proof** packaging bag which contains **desiccant** packets and a **humidity indicator** card, sealing the bag immediately, and then shipping the device to the customer in these...

...etc.).

Dry packing protects product from envirom-nental moisture by maintaining the interior of the **dry pack** bag at (less than or equal to) 20 percent RH. Included in the **dry pack** bag are a prescribed number of **desiccant** pouches. The **desiccant** pouches greatly reduce the presence of moisture.

0 SUNDAARY OF THE INVENTION
There exists a...

...invention, a carrier for a semiconductor device is provided. The carrier includes a material containing **desiccant** particles embedded therein and a holding region for the semiconductor device.

Another aspect of the present invention provides a method for manufacturing such a semiconductor **carrier** . The method includes the steps ofmixing a **desiccant** with molten **plastic** and molding the mixture into a product **carrier** .

Other objects and advantages of the present invention will become readily apparent to those skilled...

...INVENTION
An embodiment of the present invention is illustrated in Fig. 1, wherein the product **carrier** is a **tray** 20 formed from a material, e.g., **plastic** . It will be appreciated that other materials suitable for forming relatively thin, sturdy structures can...

...form tray 20. Exemplary materials include, for example, conductive thermoplastic, non-conductive and insulated plastic, **antistatically** coated PVC, **antistatically** coated polysulfone (to provide protection from **ESD** damage and to eliminate the potential for low leakage between component leads), conductive carbon-filled **polypropylene** , and black dissipative BPI-10 **plastic** . hi certain embodiments, the **carrier** material can withstand temperatures up to about 40'C to about 60'C, for example...

...C to 150'C. The material can also include a carbon-based material or be **antistatically** coated to provide **ESD** protection.

With continued reference to Fig. 1. **desiccant** particles 25 are embedded within tray 20. A preferred **desiccant** is **montmorillonite** (bentonite) clay. Tray 20 includes a notched comer 25, a flat or open bottom 27... skill in the art will appreciate that the present invention is not limited to product **carriers** for any particular **IC package** style. Rather, the product **carriers** of the present invention may be configured to accommodate, for example, Pin Grid Arrays (PGAs...

...and the sixth serving as a cover. Bound trays may then be loaded into an **antistatic** bubble pack bag, for extra cushioning protection, and then packed in a tray box for shipment.

Because a **desiccant** is incorporated directly into the product carrier, it is unnecessary to include separate **desiccant** packets in the packaging bag.

Fig. 2 is a flow diagram illustrating the method for...

...0 with an embodiment of the present invention. Referring to Fig. 2 at step 200, **desiccant** particles, such as **montmorillonite** (bentonite) clay, are mixed with molten plastic. At step 2 1 0, the molten **plastic** with **desiccant** particles mixed therein is molded into the product **carrier** , as with conventional techniques. One of ordinary skill in the art will appreciate that the amount of **desiccant** mixed with the molten plastic will be sufficient to greatly reduce the presence of moisture in a **dry pack** bag (i.e., 1 5 moisture barrier **bag**). For example, the amount of **desiccant** mixed with the molten **plastic** can be optimized such that there are about 32 grams of clay to about 64 grams of clay per **dry pack bag** .

Alternatively, the amount of **desiccant** mixed with the molten **plastic** can be optimized such that the environment in the **bag** is maintained at no greater than 20 percent RH, thus protecting the devices during shipment...

...only if the RH in the bag has exceeded 30 percent, as evidenced by a **humidity indicator** card.

Upon determination that a product is moisture sensitive , the product is dry packed for...
...type of product carrier (e.g., tubes, trays, reels, etc.).

The first step in the **dry pack** process is to remove any moisture buildup in the package by baking the finished product...

...aluminum trays or tubes. Within 50 hours after baking, the product is sealed in a **dry pack** bag under a partial vacuum.

An exemplary **dry pack** bag (i.e., moisture barrier bag) is designed with three layers. The inner layer is a low-density polyethylene, which has a **static** -dissipative coating. A second layer is 400 angstroms aluminum metallized to 92-guage polyester. 'Ihe third layer is 400 angstrom aluminum metallized to 92-guage polyester, which has a **static** -dissipative coating. **ESD** protection is provided by the inner layer of **antistatic** polyethylene and the second layer of aluminum metallized polyester.

The bag is sealed using an...

...psi; and a temperature range of about 191 to about 232'C.

Included in each **dry pack** bag is a card that has humidity sensitive elements which turn from blue to pink...

...specific RH level is exceeded.

Labels may also be applied to the outside of the **dry pack** bag. For example, a standard product label, which identifies the contents by manufacturing lot number...

...part number, and the product date code(s) and quantity per date code. Also, a **dry pack** caution label, which identifies the date the bag was sealed, the **dry pack** expiration date (which is 12 months later)), as well as product handling guidelines. A small...

Claim

I - A carrier for a semiconductor device, the carrier comprising:
a material containing a **desiccant** embedded therein; and
a holding region for the semiconductor device.

2 The carrier of claim 1, wherein the **desiccant** is **montmorillonite** (bentonite) clay.

3 The carrier of claim 1, wherein the material can withstand temperatures from...

...manufacturing a carrier for a semiconductor device, the method comprising the steps of.
mixing a **desiccant** with molten **plastic** ;
molding the mixture into a product **carrier** .
loading a device into the product carrier; and
dry packing the loaded product carrier in a bag.

9 The method of claim 8, comprising:
mixing sufficient **desiccant** with the molten **plastic** such that the dry packed product **carrier** comprises from about 32 grams of **desiccant** to about 64 grams of **desiccant** .
1 0. The method of claim 8, comprising:
mixing sufficient **desiccant** with the molten **plastic** such that an environment within the dry packed **bag** is maintained at no greater than about 20 percent relative humidity for about 12 months...

...packed bag.

15 The method of claim 8, further comprising:
labeling an outside of the **dry pack** bag;
packing the **dry pack** bag in a box; and
labeling an outside of the box with a moisture-sensitivity...

```
Set     Items   Description
S1     323008   IC OR INTEGRATED()CIRCUIT?
S2      92396   (CIRCUIT OR SILICON OR SEMICONDUCT?R OR SEMI()CONDUCT?R OR
             ELECTRONIC)()(CHIP OR CHIPS OR COMPONENT?)
S3       5400   SMD OR SURFACE()MOUNT?()DEVICE?
S4     447871   PACKAGE? OR PACK OR PACKS OR PLCC OR QFP
S5     423265   TRAY OR TRAYS OR TUBE OR TUBES
S6     519569   RECEPTACLE? OR CARRIER?
S7     281338   CONTAINER? OR BAG OR BAGS
S8     473605   ELECTROSTATIC? OR STATIC? OR ANTISTATIC? OR ESD OR ESC
S9      14914   DESSICAT? OR DESSICANT? OR DESICCAT? OR DESICCANT?
S10       281   DRIBOX OR DRI()BOX OR DRYBOX OR DRY()BOX OR DRIPACK OR DRI-
             ()PACK OR DRYPACK OR DRY()PACK OR DRIPAK OR DRI()PAK OR DRYPAK
              OR DRY()PAK
S11      5727   (MOISTURE OR HUMIDITY)()(PROOF OR ABSORB? OR ADSORB? OR AB-
             SORP? OR ADSORP?)
S12     56094   MONTMORILLONITE OR SILICA()GEL OR MOLECULAR()SIEVE?
S13     17858   CALCIUM()(OXIDE OR SULFATE) OR ACTIVATE?()ALUMIN? OR ALUMI-
             N?()SILICA?
S14      1905   (HUMIDITY OR MOISTURE)()(INDICAT?R? OR MONITOR?) OR HUMITE-
             CT? OR COBALT()CHLORIDE
S15     40417   POLY()(STYRENE OR PROPYLENE OR VINYL OR AMIDE)
S16    809597   POLYSTYRENE OR POLYPROPYLENE OR POLYMER OR POLYVINYL OR PO-
             LYAMIDE
S17    765833   ELASTOMER OR PLASTIC? ?
S18     38347   S1:S3 AND S4:S7
S19         6   S18 AND S8 AND S9:S13
S20         9   S18 AND S14
S21     38347   S18 AND S15:S18(5N)S4:S7
S22      2418   S18 AND S15:S17(5N)S4:S7
S23        87   S22 AND S8
S24         1   S23 AND (S9:S13 OR S14)
S25        15   S19:S20 OR S24
S26        15   RD (unique items)
S27        15   S26 AND PY<2003
? show files
File  94:JICST-EPlus 1985-2003/Nov W5
         (c)2003 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2003/Nov W2
         (c) 2003 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2003/Oct
         (c) 2003 The HW Wilson Co.
File  35:Dissertation Abs Online 1861-2003/Oct
         (c) 2003 ProQuest Info&Learning
File 111:TGG Natl.Newspaper Index(SM) 1979-2003/Nov 24
         (c) 2003 The Gale Group
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
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         (c) 2003 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
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         (c) 2001 THE NEW YORK TIMES
File 474:New York Times Abs 1969-2003/Nov 29
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(c) 2003 The New York Times
File 475:Wall Street Journal Abs 1973-2003/Nov 26
(c) 2003 The New York Times
File 481:DELPHES Eur Bus 95-2003/Nov W2
(c) 2003 ACFCI & Chambre CommInd Paris
File 484:Periodical Abs Plustext 1986-2003/Nov W4
(c) 2003 ProQuest

27/5,K/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04047208 JICST ACCESSION NUMBER: 99A0336175 FILE SEGMENT: JICST-E
IC **with** humidity indicator .
YAMADA MANABU (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, **1999** , VOL.17,NO.21, PAGE.101-102, FIG.2
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
DESCRIPTORS: **integrated circuit** ; surface mount technology; **IC package** ; moisture proof packaging; wrapping; humidity sensor
BROADER DESCRIPTORS: micro circuit; high density packaging; packaging(mounting); **container** ; packaging; packaging technology; hygrometer; meteorological instrument; sensor; instrumentation element
CLASSIFICATION CODE(S): NC03020K

IC **with** humidity indicator .
, **1999**
DESCRIPTORS: **integrated circuit** ; ...
... **IC package** ;
...BROADER DESCRIPTORS: **container** ;

27/5,K/2 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03560419 JICST ACCESSION NUMBER: 98A0352954 FILE SEGMENT: JICST-E
Semiconductor devices.
HARADA HIDEAKI (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, **1998** , VOL.16,NO.17, PAGE.151-152, FIG.1
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
DESCRIPTORS: **IC package** ; desiccant; **cobalt chloride** ; hygroscopic coefficient; moisture proofing; display
BROADER DESCRIPTORS: **container** ; chloride; chlorine compound; halogen compound; halide; cobalt compound; iron group element compound; transition metal compound; coefficient; soil moisture constant; constant; soil moisture property; moisture characteristic; characteristic; physical property of soil; soil property; preclusion(protection
CLASSIFICATION CODE(S): NC03020K
, **1998**
DESCRIPTORS: **IC package** ; ...

... **cobalt chloride** ;
BROADER DESCRIPTORS: **container** ;

27/5,K/3 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01784858 JICST ACCESSION NUMBER: 93A0547233 FILE SEGMENT: JICST-E
Accurate 3D Capacitance Evaluation in Integrated Capacitive Humidity Sensors.
KORVINK J G (1); CHANDRAN L (1); BOLTSHAUSER T (1); BALTES H (1)
(1) ETH-Hoenggerberg, Zuerich, CHE
Sens Mater, **1993** , VOL.4,NO.6, PAGE.323-335, FIG.7, TBL.1, REF.15
JOURNAL NUMBER: L0338AAP ISSN NO: 0914-4935 CODEN: SENME
UNIVERSAL DECIMAL CLASSIFICATION: 621.382+
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: We describe progress made towards the accurate 3-D modelling of integrated capacitive humidity microsensors fabricated using industrial CMOS technology. The designs are based on microelectrodes coated with a **moisture - absorbing** polyimide layer. A new dedicated software **package** , semiconductor sensor device simulation (SESES), has been developed for this purpose. It solves the 3-D Poisson equation over the full sensor structure, subject to appropriate boundary conditions, using the finite-element method. The solution determines the induced surface charge on the electrodes and hence the exact capacitance, which can then be used for 'dielectric modelling', namely, to assess the accuracy of various models of dielectric behaviour in the polyimide, from a comparison with experimental results. We also describe progress made in the optimization of sensor design, particularly in improving the sensitivity to humidity. We outline how SESES can also be used for the careful study of reliability considerations, such as the effects of embedded charges. Our results are relevant to integrated microsensors in general, i.e., any application involving capacitance measurements. (author abst.)
DESCRIPTORS: humidity sensor; polyimide; CMOS structure; **electrostatic** capacity; sensitivity(ratio); computer simulation; Poisson equation; finite element method; modeling; dielectric thin film; polymer membrane ; semiconductor **integrated circuit** ; surface charge
BROADER DESCRIPTORS: hygrometer; meteorological instrument; sensor; instrumentation element; polymer; MOS structure; device structure; capacity; sensitivity; property; degree; computer application; utilization; simulation; differential equation; equation; formula; approximation method; operation(processing); thin film; membrane and film; dielectrics; dielectric material; material; functional polymer; macromolecule; **integrated circuit** ; micro circuit; electric charge
CLASSIFICATION CODE(S): NC03150A
, **1993**
...ABSTRACT: microsensors fabricated using industrial CMOS technology. The designs are based on microelectrodes coated with a **moisture - absorbing** polyimide layer. A new dedicated software **package** , semiconductor sensor device simulation (SESES), has been developed for this purpose. It solves the 3...
...DESCRIPTORS: **electrostatic** capacity...

...semiconductor **integrated circuit** ;
...BROADER DESCRIPTORS: **integrated circuit** ;

27/5,K/4 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1174349 H.W. WILSON RECORD NUMBER: BAST94042956
Packaging electronics is more than damage control
Baum, Chris;
Packaging (Boston, Mass.) v. 39 (June '94) p. 24
DOCUMENT TYPE: Feature Article ISSN: 0746-3820 LANGUAGE: English
RECORD STATUS: New record

ABSTRACT: Because packaging-quality problems can affect not only a product's effectiveness but also a company's reputation, VLSI Technology turned to United Desiccants for help in packaging its sensitive circuitry. VLSI developed a vacuum-sealed, barrier **bag** to contain its Metric Quad Flat **Pack** , which holds the microprocessor chips. Six special plastic **trays** are stacked and placed into the barrier **bag** together with United Desiccants' Desi Pak moisture-adsorbing desiccant and an **SMD - Humitector** humidity-indicating card.

DESCRIPTORS: Packing for shipment; Drying agents; Electronic apparatus and instruments--Protection;

...ABSTRACT: United Desiccants for help in packaging its sensitive circuitry. VLSI developed a vacuum-sealed, barrier **bag** to contain its Metric Quad Flat **Pack** , which holds the microprocessor chips. Six special plastic **trays** are stacked and placed into the barrier **bag** together with United Desiccants' Desi Pak moisture-adsorbing desiccant and an **SMD - Humitector** humidity-indicating card.
1994

27/5,K/5 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1545395 NTIS Accession Number: DE90017595
Short and long loop manufacturing feedback using a multi-sensor assembly test chip
Sweet, J. N. ; Tuck, M. R. ; Peterson, D. W. ; Palmer, D. W.
Sandia National Labs., Albuquerque, NM.
Corp. Source Codes: 068123000; 9511100
Sponsor: Department of Energy, Washington, DC.
Report No.: SAND-90-2033C; CONF-9010158-2
1990 17p
Languages: English Document Type: Conference proceeding
Journal Announcement: GRAI9104; NSA1500
IEEE/CHMT international electronics manufacturing technology symposium (9th), Washington, DC (USA), 1-3 Oct 1990. Sponsored by Department of Energy, Washington, DC.
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NTIS Prices: PC A03/MF A01
Country of Publication: United States
Contract No.: AC04-76DP00789
A three generation family of CMOS silicon test chips for packaging diagnostics has been developed. These Assembly Test Chips (ATC) contain sensors that measure a number of variables associated with assembled **IC** degradation, including the degree of **IC** corrosion, handling damage, ESD

threat, ppm, moisture, mechanical stress, mobile ion density, bond pad cratering, and high speed logic degradation. The ATC family are intended to give manufacturing feedback in four ways: direct feedback in evaluation of an Assembly Manufacturing Line in an objective, non-intrusive way; before and after comparisons on an assembly production line when an individual process, material, or piece of equipment has been changed; resident lifetime monitor for system **package** aging and ongoing reliability projection and thermal, mechanical, dc electrical, and high frequency mock-up evaluation of packaging (including multichip) schemes. 14 refs., 6 figs., 2 tabs. (ERA citation 15:049191)

Descriptors: **Integrated Circuits** ; *Process Control; *Diagnostic Techniques; *Feedback; *Packaging; Aging; Bonding; Corrosion; Damage; Design; Electrical Properties; Fabrication; Failure Mode Analysis; Layers; Measuring Methods; **Moisture** ; **Monitoring** ; Optimization; Reliability; Specifications; Stress Analysis; Structural Models

Identifiers: *CMOS; *Computer aided manufacturing; EDB/420500; EDB/426000 ; EDB/320303; Chips(Electronics); Assembly test chips; Sensors; Feedback control; Nondestructive testing; NTISDE

Section Headings: 49H (Electrotechnology--Semiconductor Devices); 41G (Manufacturing Technology--Quality Control and Reliability); 94J (Industrial and Mechanical Engineering--Nondestructive Testing); 41B (Manufacturing Technology--Computer Aided Manufacturing (CAM))

... Assembly Test Chips (ATC) contain sensors that measure a number of variables associated with assembled **IC** degradation, including the degree of **IC** corrosion, handling damage, ESD threat, ppm, moisture, mechanical stress, mobile ion density, bond pad cratering...

... individual process, material, or piece of equipment has been changed; resident lifetime monitor for system **package** aging and ongoing reliability projection and thermal, mechanical, dc electrical, and high frequency mock-up...

Descriptors: **Integrated Circuits** ; *Process Control; *Diagnostic Techniques; *Feedback; *Packaging; Aging; Bonding; Corrosion; Damage; Design; Electrical Properties; Fabrication; Failure Mode Analysis; Layers; Measuring Methods; **Moisture** ; **Monitoring** ; Optimization; Reliability; Specifications; Stress Analysis; Structural Models

27/5,K/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04883268 E.I. No: EIP97123944852

Title: Test chip development to support standardization efforts

Author: Bright, Bill

Corporate Source: Symbios Logic, Inc, Fort Collins, CO, USA

Conference Title: Proceedings of the 1997 21st IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium

Conference Location: Austin, TX, USA Conference Date: 19971013-19971015

Sponsor: IEEE

E.I. Conference No.: 47387

Source: Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium 1997. IEEE, Piscataway, NJ, USA,97CH36068. p 184-191

Publication Year: 1997

CODEN: 61UNAI

Language: English

Document Type: CA; (Conference Article) Treatment: G; (General Review)

Journal Announcement: 9801W4

Abstract: A test chip has been developed which integrates test structures for performing reliability testing, and thermal and electrical characterization on **packages** and assembly processes. This work supports test chip standardization efforts of the Semiconductor Assembly Council (SAC) and the JEDEC JC15 Electrical Measurements and Simulation Committee. For the purpose of reliability qualifications, several single-metal structures are provided to evaluate the environmental integrity of the **package** . Characterization structures, such as a capacitor for **moisture monitoring** , a strain gauge rosette, diodes, a heating resistor, and custom digital drivers have been integrated to quantify the mechanical, thermal, and electrical performance aspects of the **package** . This paper provides an overview of the test die functionality and discusses the application of each test sensor. (Author abstract) 10 Refs.

Descriptors: Electronics packaging; **Integrated circuit** testing; Standardization; Reliability; **Integrated circuit** manufacture; Capacitors; Moisture determination; Strain gages; Resistors; Dies

Identifiers: Reliability testing; Strain gage rosettes

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 902.2 (Codes & Standards); 913.3 (Quality Assurance & Control); 704.1 (Electric Components)

714 (Electronic Components); 902 (Engineering Graphics & Standards); 421 (Materials Properties); 913 (Production Planning & Control); 704 (Electric Components & Equipment)

71 (ELECTRONICS & COMMUNICATIONS); 90 (GENERAL ENGINEERING); 42 (MATERIALS PROPERTIES & TESTING); 91 (ENGINEERING MANAGEMENT); 70 (ELECTRICAL ENGINEERING)

...Abstract: developed which integrates test structures for performing reliability testing, and thermal and electrical characterization on **packages** and assembly processes. This work supports test chip standardization efforts of the Semiconductor Assembly Council...

...reliability qualifications, several single-metal structures are provided to evaluate the environmental integrity of the **package** . Characterization structures, such as a capacitor for **moisture monitoring** , a strain gauge rosette, diodes, a heating resistor, and custom digital drivers have been integrated to quantify the mechanical, thermal, and electrical performance aspects of the **package** . This paper provides an overview of the test die functionality and discusses the application of...

Descriptors: Electronics packaging; **Integrated circuit** testing; Standardization; Reliability; **Integrated circuit** manufacture; Capacitors; Moisture determination; Strain gages; Resistors; Dies

27/5,K/7 (Item 2 from file: 8)

01025272 E.I. Monthly No: EI8106048462 E.I. Yearly No: EI81034333

Title: RECENT ADVANCES IN Al//2O//3 " IN-SITU " MOISTURE MONITORING **CHIPS FOR CERDIP** PACKAGE **APPLICATIONS.**

Author: Finn, J. B.; Fong, V.

Corporate Source: Mostek Corp, Carrollton, Tex

Source: Annu Proc Reliab Phys Symp 18th, Las Vegas, Nev, Apr 8-10 1980. Publ by IEEE (Cat n 80CH1531-3), Piscataway, NJ, 1980 p 10-16

Publication Year: 1980

CODEN: ARLPBI ISSN: 0099-9512

Language: ENGLISH

Journal Announcement: 8106

Abstract: Determination of the internal water vapor of a Cerdip **package** can be conveniently and inexpensively performed by an Al//2O//3 chip type sensor of recent design. Comparisons with an earlier design are made. Data of field trials by several **IC** manufacturers from common chip lots are shown. For the purpose of generating a broad range of moisture levels, both vitreous and nonvitreous sealing glass types were studied along with the effect of desiccants, lint contamination of the sealing glass, and the leak detection capability of the sensor. The relationship of sensor measured values with those of mass spectrometry is shown. 7 refs.

Descriptors: *ELECTRONICS PACKAGING--*Moisture Control; SENSORS

Classification Codes:

715 (General Electronic Equipment); 944 (Moisture, Pressure & Temperature, & Radiation Measuring Instruments)

71 (ELECTRONICS & COMMUNICATIONS); 94 (INSTRUMENTS & MEASUREMENT)

Title: RECENT ADVANCES IN Al//2O//3 " IN-SITU " MOISTURE MONITORING **CHIPS FOR CERDIP** PACKAGE **APPLICATIONS.**

Abstract: Determination of the internal water vapor of a Cerdip **package** can be conveniently and inexpensively performed by an Al//2O//3 chip type sensor of recent design. Comparisons with an earlier design are made. Data of field trials by several **IC** manufacturers from common chip lots are shown. For the purpose of generating a broad range...

27/5,K/8 (Item 3 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

00895530 E.I. Monthly No: EI8002013051 E.I. Yearly No: EI80045513

Title: CHARACTERISTICS OF A SURFACE CONDUCTIVITY MOISTURE MONITOR **FOR HERMETIC** INTEGRATED CIRCUIT PACKAGES .

Author: Lowry, Robert K.; Miller, L. A.; Jonas, Allen W.; Bird, J. M.

Corporate Source: Harris Semicond, Melbourne, Fla

Source: Annu Proc Reliab Phys Symp 17th, San Francisco, Calif, Apr 24-26 1979. Publ by IEEE (Cat n 79CH1425-8PHY), New York, NY, 1979 p 97-102

Publication Year: 1979

CODEN: ARLPBI ISSN: 0099-9512

Language: ENGLISH

Journal Announcement: 8002

Abstract: An in-situ surface conductivity sensor for measuring water content of hermetic **package** ambients is described. Results of correlation experiments with mass spectroscopy and volume-effect sensors are presented. Sensor studies of water desorption and contamination by leached ions are discussed. The surface conductivity sensor is well-suited to defining moisture levels within all types of hermetic **packages** . 19 refs.

Descriptors: **INTEGRATED CIRCUITS** --*Packaging; RELIABILITY

Classification Codes:

714 (Electronic Components); 713 (Electronic Circuits); 913 (Production Planning & Control); 421 (Materials Properties)

71 (ELECTRONICS & COMMUNICATIONS); 91 (ENGINEERING MANAGEMENT); 42 (MATERIALS PROPERTIES & TESTING)

Title: CHARACTERISTICS OF A SURFACE CONDUCTIVITY MOISTURE MONITOR **FOR HERMETIC** INTEGRATED CIRCUIT PACKAGES .

Abstract: An in-situ surface conductivity sensor for measuring water content of hermetic **package** ambients is described. Results of correlation experiments with mass spectroscopy and volume-effect sensors are...

...surface conductivity sensor is well-suited to defining moisture levels within all types of hermetic **packages** . 19 refs.

Descriptors: **INTEGRATED CIRCUITS** --*

27/5,K/9 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00393191 E.I. Monthly No: EI7409058752
Title: NEW SIMPLIFIED METHOD TO MEASURE MOISTURE IN MICRO ENCLOSURES.
Author: Zatz, Saul
Corporate Source: Martin Marietta Aersop, Orlando, Fla
Source: Electron Components Conf, 24th, Proc, Washington, DC, May 13-15 1974 p29-33. Available from IEEE, New York, 1974
Publication Year: 1974
Language: ENGLISH
Journal Announcement: 7409
Abstract: A new technique has been perfected to accurately measure the moisture content in the small volumes typified by semiconductor and **integrated circuit packages** . The methodology uses an inexpensive, easily fabricated **moisture monitor** that incorporates two bond wires in a standard **package** . After **package** seal as part of a production seal run, the dew point can be directly and accurately measured. A recognized direct relationship exists between dew points and moisture content. Comparison with other techniques and life tests of moisture sensitive parts have demonstrated the validity and effectiveness of this approach. The new technique eliminates the gross errors that are introduced when the micro-volume is drawn into a large volume test manifold. This technique is currently being used to certify the process controls and seal effectiveness of critical **integrated circuits** for a high reliability system. 5 refs.
Descriptors: *SOLID STATE DEVICES--*Electronics Packaging
Classification Codes:
714 (Electronic Components)
71 (ELECTRONICS & COMMUNICATIONS)

...Abstract: perfected to accurately measure the moisture content in the small volumes typified by semiconductor and **integrated circuit packages** .. The methodology uses an inexpensive, easily fabricated **moisture monitor** that incorporates two bond wires in a standard **package** . After **package** seal as part of a production seal run, the dew point can be directly and...

...technique is currently being used to certify the process controls and seal effectiveness of critical **integrated circuits** for a high reliability system. 5 refs.

27/5,K/10 (Item 1 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

05593594 SUPPLIER NUMBER: 127089781 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Framing and flattering works of art on paper
Grant, Daniel
Consumers' Research Magazine (GCRM), v85 n5, p24-28, p.5
May 2002
ISSN: 0095-2222 JOURNAL CODE: GCRM
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 3893

ABSTRACT: The subject of framing of works of art occupies a lot of time for art dealers and even more for collectors. Two issues face collectors in displaying works on paper, and they are sometimes treated as mutually exclusive.

DESCRIPTORS: Collectors; Art; Picture framing
CODEN: CRMZA6

2002
TEXT:
... buy and for how much.

Most museums these days have quite high-tech temperature and **humidity monitoring** systems controlling the interior environment. That kind of control is less possible where people live...wide.

Conservators speak not only about framing and matting but also about the entire "frame **package** ." That **package** typically consists of backing material, a backboard, the drawing itself, a window mat, covering glass... Works, 1717 K Street, N.W., Washington, DC 20006,202-452-9545, www.aic-fa.**ic** .org.

Daniel Grant

Mr. Grant is the author of several books on art, including The...

27/5,K/11 (Item 2 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

04500517 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Let's network some more
Fleck, Ken
Electronic News (IELN), v45 n40, p40, p.1
Oct 4, 1999
ISSN: 1061-6624 JOURNAL CODE: IELN
DOCUMENT TYPE: Commentary
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 577

ABSTRACT: Fleck examines trends in packaging and high-speed digital circuitry, which are design challenges faced by the connector industry and new connector designs.

DESCRIPTORS: Packaging; **Integrated circuits**
SPECIAL FEATURES: Photograph

1999

TEXT:
... Calif., now is offering its miniature wafer-level chip-scale packaging (CSP) technology, termed micro **SMD** , with an additional 13 of its analog products.

The semiconductors introduced last week target applications...

...size or weight constraints such as handheld and portable products. National first used the micro **SMD** technology a year ago to **package** a dual op amp.

"The 8-10 version of this new **package** occupies 85 percent less surface area than an 8-lead MSOP," said Pat Brockett, executive...

...SMDs. Thus, designers will be able to execute a complete system design using these tiny **packages** ."

And the firm noted "since it is a wafer-level packaging process, a whole series...

...process."

A patented encapsulation process on the front and back of the wafer produces a **packageless** device. Micro **SMD** products conform to standard JEDEC pinout patterns, assuring accurate circuit board placement using existing mounting equipment. Customers can transition to micro **SMD** parts without any retooling of their standard surface mount manufacturing equipment, National added.

"We tested the new micro **SMD** from National Semiconductor on Universal Instruments' GSM pick-- and-place system," said Jayson Noland, senior...

...Silicon Valley Technology Center we were able to pick, inspect and accurately place the micro **SMD** components with ease."

National also claimed micro **SMD** packaging yields more reliable components.

"Shorter interconnections result in low inductance and minimal signal degradation; micro **SMD - packaged** components actually meet or beat standard electrical characteristics. Micro **SMD packages** meet the level-1 specification for moisture sensitivity. No **dry pack** , nitrogen storage or bake is required. National's micro **SMD package** passed all mechanical and electrical tests, thermal cycles, solderjoint integrity, **ESD** , vibration and drop tests with zero failures. Moreover, unlike some surface mount **packages** , no underfill is required, simplifying and reducing production costs."

Today, National is delivering the LMC555...

...DESCRIPTORS: **Integrated circuits**

27/5,K/12 (Item 3 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

04500516 (USE FORMAT 7 OR 9 FOR FULLTEXT)
National hikes wafer-level CSP use
Anonymous
Electronic News (IELN), v45 n40, p40, p.1
Oct 4, 1999
ISSN: 1061-6624 JOURNAL CODE: IELN
DOCUMENT TYPE: News
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 577

ABSTRACT: National Semiconductor Corp is offering its miniature wafer-level chip-scale packaging technology with an additional 13 of its analog products. The technology is called micro **SMD** .

DESCRIPTORS: Semiconductors; Packaging
SPECIAL FEATURES: Illustration
COMPANY INFORMATION:
National Semiconductor Corp

1999
...ABSTRACT: packaging technology with an additional 13 of its analog

products. The technology is called micro **SMD** .
TEXT:
... Calif., now is offering its miniature wafer-level chip-scale packaging (CSP) technology, termed micro **SMD** , with an additional 13 of its analog products.
The semiconductors introduced last week target applications...

...size or weight constraints such as handheld and portable products. National first used the micro **SMD** technology a year ago to 1package a dual op amp.
"The 8-I/O version of this new **package** occupies 85 percent less surface area than an 8-lead MSOP," said Pat Brockett, executive...

...SMDs. Thus, designers will be able to execute a complete system design using these tiny **packages** ."
And the firm noted "since it is a wafer-level packaging process, a whole series...

...process."
A patented encapsulation process on the front and back of the wafer produces a **packageless** device. Micro **SMD** products conform to standard JEDEC pinout patterns, assuring accurate circuit board placement using existing mounting equipment. Customers can transition to micro **SMD** parts without any retooling of their standard surface mount manufacturing equipment, National added.
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...Silicon Valley Technology Center we were able to pick, inspect and accurately place the micro **SMD** components with ease."
National also claimed micro **SMD** packaging yields more reliable components.
"Shorter interconnections result in low inductance and minimal signal degradation; micro **SMD** - **packaged** components actually meet or beat standard electrical characteristics. Micro **SMD** **packages** meet the level-1 specification for moisture sensitivity. No **dry** **pack** , nitrogen storage or bake is required. National's micro **SMD** **package** passed all mechanical and electrical tests, thermal cycles, solder joint integrity, **ESD** , vibration and drop tests with zero failures. Moreover, unlike some surface mount **packages** , no underfill is required, simplifying and reducing production costs."
Today, National is delivering the LMC555...

27/5,K/13 (Item 4 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

03448960 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Magnetic field alignment of ordered silicate-surfactant composites and mesoporous silica
Tolbert, Sarah H; Firouzi, Ali; Stucky, Galen D; Chmelka, Bradley F
Science (GSCI), v278 n5336, p264-268, p.5
Oct 10, 1997
ISSN: 0036-8075 JOURNAL CODE: GSCI
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 4016

ABSTRACT: Macroscopic orientational ordering of the pores of condensed hexagonal mesostructured silica was achieved through alignment of an unpolymerized, hexagonal, lyotropic silicate-surfactant liquid cyrstal in a high magnetic field.

DESCRIPTORS: Materials science; Chemistry; Magnetism; Silicon
SPECIAL FEATURES: References Graph Illustration Photograph

1997
TEXT:
... to consist of aggregates of assembled surfactant molecules that interact covalently (3, 8, 10) or **electrostatically** (1, 6, 8) with an inorganic framework. For densely cross-linked inorganic mesostructures, it is...

...separations, and chemical sensing of molecules that are too large for processing with crystalline zeolite **molecular sieves** , which generally have smaller (2 to 15 Angstrom) micropores. Mesoporous solids may also be usedshow that the spectrum in Fig. **IC** can be reproduced from a model in which 80% of the cetyltrimethylammonium ions (CTA+) reside...

...silicate-surfactantrich phase, and the latter was exposed to concentrated HCI vapor in a closed **container** for 1 to 3 days at room temperature (27). After removal from the acid vapor...

...the results obtained from sup 2 H NMR on the aligned liquid crystalline precursor (Fig. **IC**), indicating that long-range orientational ordering of the mesophase domains was not disrupted by polymerization...

27/5,K/14 (Item 5 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

03082700 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Narrativity, myth, and metaphor: Louise Erdrich and Raymond Carver talk about love
Downes, Margaret J
MELUS (PMEL), v21 n2, p49-61, p.13
Summer 1996
ISSN: 0163-755X JOURNAL CODE: PMEL
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5340

ABSTRACT: Downes argues that love and narrative are similarly structured experiences. A narrative involves the reader with something more or less unfamiliar or elusive, something like love, and tells about it. Her discussion of Erdich and Carver is admittedly idiosyncratic and interesting.

DESCRIPTORS: Love; Literary criticism; Novels; Metaphor
NAMED PERSONS: Erdich, Louise; Carver, Raymond
SPECIAL FEATURES: References

1996

TEXT:
... Harvard Medical School, remarks that "the brain works associatively. High-level associations are metaphors, which **pack** lots of material into an economic unit" (qtd. in Begley 44). Hobson is speaking here ...hereditary means of imposing psychological tyranny. But by myth I do not mean a monolithic, **static** and oppressive force which "fetter[s] linguistic consciousness" and exerts "absolute hegemony.. .over language" (Bakhtin...

...however, as variable and dynamic as are meaning and language. Those cultural myths which are **static** support savage societies which practice (in whatever form) ritual sacrifice. Such a society is essentially...

...myth because experience seems to pattern itself, and we cannot grasp experience unless it is **packaged** so. "Truth"-an evanescent thingis revealed when we discover and apply an appropriate structure, oftentimes... it talked out. After a time, she quit trying" (10). A late bloomer in her **desiccated** society, she finally has learned the futility, in that milieu, of trying to construct and...Recovering the Feminine in American Indian Traditions. Boston: Beacon, 1986.

Bakhtin, M. M. The Dialog- **ic** Imagination: Four Essays by M. M. Bakhtin. Ed. Michael Holquist. Trans. Caryl Emerson and Michael...

27/5,K/15 (Item 6 from file: 484)
DIALOG(R)File 484:Periodical Abs Plustext

02218369 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Engineering for the ends of the Earth
Valenti, Michael
Mechanical Engineering (GMEE), v116 n12, p56-60, p.5
Dec 1994
ISSN: 0025-6501 JOURNAL CODE: GMEE
DOCUMENT TYPE: Feature
LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2993 LENGTH: Long (31+ col inches)

ABSTRACT: Scientists are using meteorological and oceanographic instruments, including thermistors and snow depth sensors, designed to withstand harsh conditions to study polar climates. The instruments are sensitive to the slightest variations in temperature, pressure, moisture and wind speed but can withstand harsh weather.

DESCRIPTORS: Instruments; Climate; Meteorology; Research & development; R&D
SPECIAL FEATURES: Photograph
1994

TEXT:
... Project.

Engineers get around this problem in two ways, Zika explained: by locating the battery **packs** of their polar research systems out of the wind and as close to sea level...

...mounted on a pipe extended from a tower, is suspended over the snow. An ultrasonic **electrostatic** transducer emits 50 kHz sound pulses that bounce back to the sensor and are timed...pass through, and a closed piping system that interconnects the barometer and water trap with **desiccant** chambers

containing **silica gel** to keep the air dry.

The Ice Platform measures the air temperature with a thermistor contained in a watertight **tube** fixed inside the mast's radiation shield. This shield permits air to flow freely around...ice damage. This tubing also relieves strain should the buoy drift free from the ice **pack** in case the **pack** breaks up. **Polyvinyl** chloride tubing above the pressure sensor also provides strain relief on the bottom end of...

...sensing cable.

D-cell batteries made of alkaline-manganese dioxide power the Ice Platform battery **pack** because these yield greater capacity and low-temperature performance than standard retail batteries. The battery **pack** consists of 16 groups of 12 (nominally 18 volts each) wired in parallel via isolating diodes. This configuration prevents accidental self-discharge of the **pack** if any battery stick fails. Data acquisition and processing units collect the analog signals from...

...6061-T6 aluminum alloy. This alloy, originally developed by aerospace manufacturers, strengthens the buoy's **electronic components** ' resistance to high-frequency radio waves and protects them from the crushing effects of moving...

```
Set     Items   Description
S1     467663   IC OR INTEGRATED()CIRCUIT?
S2     494627   (CIRCUIT OR SILICON OR SEMICONDUCT?R OR SEMI()CONDUCT?R OR
           ELECTRONIC)()(CHIP OR CHIPS OR COMPONENT?)
S3      11690   SMD OR SURFACE()MOUNT?()DEVICE?
S4    4039519   PACKAGE? OR PACK OR PACKS OR PLCC OR QFP
S5     572586   TRAY OR TRAYS OR TUBE OR TUBES
S6    3144263   RECEPTACLE? OR CARRIER?
S7    1349237   CONTAINER? OR BAG OR BAGS
S8     302428   ELECTROSTATIC? OR STATIC? OR ANTISTATIC? OR ESD OR ESC
S9       9936   DESSICAT? OR DESSICANT? OR DESICCAT? OR DESICCANT?
S10       632   DRIBOX OR DRI()BOX OR DRYBOX OR DRY()BOX OR DRIPACK OR DRI-
           ()PACK OR DRYPACK OR DRY()PACK OR DRIPAK OR DRI()PAK OR DRYPAK
            OR DRY()PAK
S11      4534   (MOISTURE OR HUMIDITY)()(PROOF OR ABSORB? OR ADSORB? OR AB-
           SORP? OR ADSORP?)
S12      6227   MONTMORILLONITE OR SILICA()GEL OR MOLECULAR()SIEVE?
S13      4648   CALCIUM()(OXIDE OR SULFATE) OR ACTIVATE?()ALUMIN? OR ALUMI-
           N?()SILICA?
S14       879   (HUMIDITY OR MOISTURE)()(INDICAT?R? OR MONITOR?) OR HUMITE-
           CT? OR COBALT()CHLORIDE
S15      1774   POLY()(STYRENE OR PROPYLENE OR VINYL OR AMIDE)
S16    378458   POLYSTYRENE OR POLYPROPYLENE OR POLYMER OR POLYVINYL OR PO-
           LYAMIDE
S17   2099715   ELASTOMER OR PLASTIC? ?
S18     24786   S1:S3(10N)S4:S7
S19        61   S18 AND S8 AND S9:S13
S20         5   S19 AND S14
S21        39   S19 AND S15:S17
S22      2711   S18 AND S15:S17(10N)S4:S7
S23       319   S22 AND S8:S14
S24        25   S23 AND (S19 OR S39)
S25        25   S23 AND (S29 OR S21)
S26        25   S23 AND (S19 OR S21)
S27        28   S20 OR S24:S26
S28        22   RD (unique items)
S29        20   S28 AND PY<2003
? show files
File   9:Business & Industry(R) Jul/1994-2003/Nov 26
         (c) 2003 Resp. DB Svcs.
File  16:Gale Group PROMT(R) 1990-2003/Nov 26
         (c) 2003 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2003/Nov 26
         (c) 2003 The Gale group
File  80:TGG Aerospace/Def.Mkts(R) 1986-2003/Nov 26
         (c) 2003 The Gale Group
File 141:Readers Guide 1983-2003/Oct
         (c) 2003 The HW Wilson Co
File 148:Gale Group Trade & Industry DB 1976-2003/Nov 27
         (c)2003 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 482:Newsweek 2000-2003/Nov 26
         (c) 2003 Newsweek, Inc.
File 621:Gale Group New Prod.Annou.(R) 1985-2003/Nov 27
         (c) 2003 The Gale Group
File 635:Business Dateline(R) 1985-2003/Nov 27
         (c) 2003 ProQuest Info&Learning
File 636:Gale Group Newsletter DB(TM) 1987-2003/Nov 26
         (c) 2003 The Gale Group
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File 646:Consumer Reports 1982-2003/Oct

File 609:Bridge World Markets 2000-2001/Oct 01

File 649:Gale Group Newswire ASAP(TM) 2003/Nov 24

File 610:Business Wire 1999-2003/Dec 01

File 613:PR Newswire 1999-2003/Dec 01

File 810:Business Wire 1986-1999/Feb 28

File 813:PR Newswire 1987-1999/Apr 30

File 20:Dialog Global Reporter 1997-2003/Dec 01

File 570:Gale Group MARS(R) 1984-2003/Nov 27

File 929:Albuquerque Newspapers 1995-2003/Nov 29

t 29/5,k/3,4,6,7,9,11

29/5,K/3 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07379217 Supplier Number: 60048603 (USE FORMAT 7 FOR FULLTEXT)
Logic IC **Market &** Packages .
SMT Trends, p1
Sept, 1998
ISSN: 0890-7900
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 26168
PUBLISHER NAME: New Insights
INDUSTRY NAMES: BUSN (Any type of business); ELEC (Electronics)

(USE FORMAT 7 FOR FULLTEXT)
Logic IC **Market &** Packages .
TEXT:
A friend called us up and asked what was going on in the logic **IC** markets. Specifically, our friend asked, what **packages** are going to be used and how many pins will these packages have.?
... electronic product design is at the place where it has to push upstream, toward the **IC** itself. The **IC** **package** is the printed circuit board of the future. These "systems" on a chip will then...ADC, and it isn't a low impedance line, it could cause considerable clock jitter. **Static** timing analysis (provided in the Synopsys toolset) is used to find such problems.

From a...with CMOS VLSI chips, he said.

Another significant breakthrough is the advent of high performance **plastic** fiber. Graded-index fibers made from per-fluorinated polymers have realized a 200-times improvement in bandwidth loss over previous **plastic** -fiber technology and could cut interconnect costs by a factor of 10, Husain said. The...been complicated by semiconductor advances such as increasing bus widths, faster clock speeds and diminishing **IC** **package** size.

Solving the Connection Problem As chip designers **pack** more functionality into ICs, spacings, sometimes as tight as 0.65 or 0.5 mm...a way to probe three or eight signals on 0.5 and 0.65 mm **IC** **packages** . The adapter features compressible "conductors" that are inserted into the spaces between the IC pins...the die itself. Additional products are expected to appear later in National's new Micro- **SMD** **package** . National's LMC6O35IBP is a general purpose dual op amp optimized for low power applications...

...to others, but no deals have yet been reached. In addition to op amps, other **IC** categories expected to follow in National's Micro- **SMD** **package** include regulators, timers, A/D converters, temperature sensors and comparators.

Fujitsu Trims Relay Package by...plane expansion mismatch between the substrate and silicon chips. Organic substrates, such as FR-4, **polyamide** and flexible polyester, are used for special assembly applications.

Chips Process development required mounting and...competitive solutions to this unheralded challenge.

Second is the tension between ultrafine-pitch quad flat **packs** (QFPs) and ball grid array (EGA) **packages** . Approximately 7 billion **plastic** OFPs will be placed in 1995, yet ultrafine-pitch (0.3 to 0.4 mm... Currently, a turret style chipshooter can place about 250 chips/sq. ft/hr. in floor.

Plastic quad flat **packs** (PQFPs) are clearly dominating the market for **IC** (**integrated circuit**) packaging, with a total of approximately seven billion used in 1995. At higher lead counts...

...can be defined.

A further advantage of multichip modules is that since they combine several **semiconductor chips** in one **package** , they allow the integration of several chip processing technologies into one circuit package. For example...

...to 70 mm wide tape consists of two or three layers of copper, adhesive, or **plastic** . The tape has a series of holes, or windows; onto each window is attached an...as increased I/O.

Chip on Board (COB) is the Emperor's New Clothes of **IC** packaging - it's no **package** at all. The **IC** die is placed directly onto the board substrate during assembly of the circuit.

COB is...

...COB has been the reluctance of chip manufacturers to ship ICs out the door without **packages** . **Packages** provide isolation and protection for the ICs, and IC manufacturers make money on the **packages** .

Test and inspection of COB present problems associated with the lack of package leads, the...

...standard EIA 583. This standard relates to the problem of damage caused to SMDs from **moisture adsorbed** during shipping and storage. Moisture can cause the IC to crack or otherwise deteriorate in integrity or performance. The EIA proposal recommends the use of **moisture adsorbing desiccant** packets, moisture sensors, and special packing materials.

Wave soldering is the general approach to through...

...than vapor phase due to these advantages.

The heat management problem poses rigorous challenges to **integrated circuit package** designers. Smaller, more powerful, denser **integrated circuits** make the problem a packaging problem as we enter the submicron era in microelectronic.

Cooling...

...has generated the most acceptance among SMT designers through 1991. The J-bend, or SOJ, **package** has leads which bend down and under the **IC** , saving precious board space and leading to a sturdy lead connection. The alternative gull-wing SO has leads which extend away from the **IC** , allowing easier inspection and better thermal dissipation for the **packaged** unit.

The need for higher pin counts in ICs drives packaging innovation. The DIP package...

...board and multichip module level.

The delays associated with electrical transmission between ICs and through **IC packages** are becoming more significant. Further improvements at the high end will likely require optical solutions...

...and area required for a specific logic function.

Many future semiconductor systems will integrate several **semiconductor chips** into one **package** , allowing the combination of several chip processing technologies into one circuit package. Systems involving digital...COB has been the reluctance of chip manufacturers to ship ICs out the door without **packages** . **Packages** provide isolation and protection for the ICs and **IC** manufacturers make money on the **packages** .

Test and inspection of COB present problems associated with the lack

of package leads, the...usually with a minimum thickness of 10 microns. Preferred materials must exhibit low dielectrics, low **moisture absorption** , planarizing capabilities, and high thermal stability to accommodate subsequent processing.
Traditionally, morganic materials have been...

...cracks and discontinuities. Polymers bring certain advantages with them when used as dielectrics in advanced **packages** . Although no one commercial **polymer** is currently able to meet all requirement s, polyimides have received a great deal of...melting range are favorable to the wave soldering process. For single sided circuit boards, the **plastic** melting range of 60/40 alloy helps the solder bridge across larger holes with small ...the process occur over the course of an entire day with assured solvent evaporation and **moisture absorption** , etc. Would it not be more sensible to try to produce a solderpaste which will...6

Units(M) 466.9 648.2 1261.4
Year 1997 1999 2003
World Logic **IC** Market By **Package** Type 1997-2003 Units (M)
SO 140.1 157.5 201.1
QFP 116.7...

...263.0
Total 466.9 648.3 1261.4
Year 1997 1999 2003
World Logic **IC** Market By **Package** Type 1996-2003 Units (M)
8 - 32 70.0 78.8 100.6
32 - 132...
19980901

29/5,K/4 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03205278 Supplier Number: 44393672 (USE FORMAT 7 FOR FULLTEXT)
United Desiccants dry pack **systems protects SMDs from moisture damage**
Electronic Chemicals News, v9, n2, pN/A
Jan 30, 1994
ISSN: 0886-5671
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 194
PUBLISHER NAME: Chemical Week Associates
COMPANY NAMES: United **Desiccants**
EVENT NAMES: *330 (Product information)
GEOGRAPHIC NAMES: *1USA (United States)
PRODUCT NAMES: *3295040 (Absorbent Clay Products)
INDUSTRY NAMES: BUSN (Any type of business); CHEM (Chemicals, Plastics and Rubber)
NAICS CODES: 327992 (Ground or Treated Mineral and Earth Manufacturing)
SPECIAL FEATURES: COMPANY

(USE FORMAT 7 FOR FULLTEXT)
United Desiccants dry pack **systems protects SMDs from moisture damage**
TEXT:

United **Desiccants** is marketing **Dry Pack** systems, which it says offers moisture protection for SMDs during shipping storage. **Dry Pack** includes an **antistatic** barrier **bag** , a Desi-Pak **moisture - adsorbing dessicant** , and an **SMD - Humitector** humidity indicating card. The barrier **bag** and **desiccant** protect the sensitive SMDs. The **SMD - Humitectot** , developed specifically for use in the electronics industry, is placed in the sealed **container** with the Desi-Pak. This **humidity indicator** card protects **electronic components** by letting users know when the atmosphere around the electrical device reaches 10, 20, 30 and 40% relative humidity and when the **desiccant** has reached its **moisture adsorption** capacity.
... changes from blue to pink if the atmosphere reaches an "unsafe" level or if insufficient **desiccant** is being used. **Humidity indicators** also allow each **package** to be visually inspected, to ensure that the **SMD** is dry and ready for soldering without decohesion of the plastic from the underside of the leadframe die pad. Desi-Pak **desiccants** and the SMD-**Humitector** should be used intandem for best results.
For more information on **Dry Pack** Electronics applications contact: Don Lawson Humidial, PO Box 610, 465 Mount Vernon Ave., Colton, CA
...
COMPANY NAMES: United **Desiccants**
19940130

29/5,K/6 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

13508616 SUPPLIER NUMBER: 75433257 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Packaging solves "the last centimeter".(Technology Information)
Israelsohn, Joshua
EDN, 46, 12, 73
May 24, 2001
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 3808 LINE COUNT: 00327

INDUSTRY CODES/NAMES: BUSN Any type of business; ELEC Electronics
DESCRIPTORS: Semiconductor chips--Design and construction
FILE SEGMENT: TI File 148

... newer TO-273 dispenses with the TO-220's bolt hole and thereby extends the **plastic package** to near the top of the metal tab. This modification makes room for a larger...

...the MOS switch, the power dissipation derives to first order from the sum of the **static** (I.sup.2)R loss and the dynamic losses associated with charging and discharging the...

...not the packaging engineer's only technology that improves small power-MOS performance. Other small **plastic package** designs minimize their footprints by limiting the extent that leads protrude from the package body...each protect four data lines from 15-kV air-discharge and 8-kV contact-discharge **ESD** strikes to comply with IEC 61000-4-2 Level 4. Compared with SOT23-6 packaged...

...significantly smaller packages and build on existing equipment, fixturing, and process recipes developed for traditional **plastic** packaging. This feature reduces the risks and costs associated with developing and qualifying new packages...series inductance
FEA: finite-element array

FPGA: fine pitch-grid array
LLP: leadless lead-frame **package**
NSMD: non-solder mask defined
RFIC: radio-frequency **integrated circuit**
SOP: small-outline **package**
SMD : solder mask defined
SMT: surface-mount technology
TCE: thermal coefficient of expansion
TFP: thin flat...packaging technologies, the higher temperatures challenge a chip maker's ability to ensure that their **plastic** components meet JEDEC moisture-sensitivity levels 1 and 2 (Reference C and Table A). Based...

...OEMs.

TABLE A--JEDEC MOISTURE-SENSITIVITY LEVELS

JEDEC moisture-sensitivity level	Floor life after opening **dry pack**
1	Unlimited(*)
2	One year
2A	Four weeks
3	Seven days
4	72 hours

(*) No **dry - pack** required

REFERENCES

(A.) "What's driving the move to lead-free solder processes," National Semiconductor...

...PCB real estate with chip scale packaging," Xcell Journal, Spring 2001, pg 34.

(5.) "Micro **SMD** wafer level chip scale **package** ," Application note 1112, National Semiconductor, November 2000.

(6.) Mescher, Paul, C Scanlan, R Erich, C...

20010524

29/5,K/7 (Item 3 from file: 148)

12517755 SUPPLIER NUMBER: 64423585 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Minimizing failures in electronic systems by design.(Technology Information)

Lakshminarayanan, V

EDN, 45, 16, 87
August 3, 2000
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 7937 LINE COUNT: 00826

INDUSTRY CODES/NAMES: BUSN Any type of business; ELEC Electronics
DESCRIPTORS: Computer peripherals industry--Product development; Testing and measuring equipment industry--Product development; Circuit components --Design and construction; System design--Technique
PRODUCT/INDUSTRY NAMES: 3825200 (Electronic Test & Measure Eqp); 3670000 (Electronic Components)
EVENT CODES/NAMES: 331 Product development
SIC CODES: 3825 Instruments to measure electricity; 3670 Electronic

Components and Accessories
NAICS CODES: 334515 Instrument Manufacturing for Measuring and Testing Electricity and Electrical Signals; 3359 Other Electrical Equipment and Component Manufacturing
FILE SEGMENT: TI File 148

... because they are sometimes undetectable and lead to field failures of equipment under operating conditions. **Electrostatic** discharge is a common cause of latent damage to electronic components.

You can explain semiconductor...

...during use,

	entry of moisture, flux, or contaminants
Mechanical stress cracks	Differential thermal expansion of **plastic** encapsulation, metal leads, or die.
Snapping of bond wires in a...	EOS or thermal shock

...in a device

Voids in the device	Chip-substrate attachment failure, thermal overstress
Metallization damage	**ESD** , corrosion, EOS, temperature
Cracks at the bond-pad-wire junction	EOS
Electromigration	Current flow
Oxide-layer faults	**ESD** , pinhole due to etching defects or impurities
Crystal defects	Bulk semiconductor-material defects
Layer misalignments...	

...seal

Melting of contacts	EOS (high current)
Damage to coil	EOS (high current)
Damage to **plastic** case	High temperature during soldering or electrical-stress-induced thermal overstress during use

PC boards...

...The factors that most commonly cause component failure in electronic circuits are EOS (electrical overstress), **ESD** (**electrostatic** discharge) and EMI, and thermal overstress. Each of these categories warrants a thorough discussion.

EOS...short circuit, which further leads to burnouts or charring of the component due to overheating.

ESD AND EMI

Recently, electronic chip and system designers have taken interest in **ESD** and EMI. The rapid proliferation of small, portable electronic gadgets, switching power supplies, and wireless transmitters and receivers have increased the problem of **ESD** and EMI effects. The miniaturization of electronic components has increased the risk factor for failures from **ESD** and EMI.

ESD occurs because of the transfer of electrons by triboelectric charging--for example, the pins of an **IC** sliding down a **tube** charge due to friction. When a charged object or person comes into contact with a...

...can charge that person to a high potential. Higher humidity conditions reduce the effect of **static** charges by providing a discharge path to ground for accumulated charges. Thus, dry air conditions tend to aggravate **ESD** problems, and higher humidity conditions reduce charge accumulation.

For **ESD** to have any effect, a source of **ESD** and a receptor must be present. In general, a source of **ESD** can be manmade or natural, and the receptor can be any component. The action of an **ESD** -induced **electrostatic** field may indirectly affect a component.

ESD REQUIRES A SOURCE AND A RECEPTOR

ESD can cause hardware and software damage in the following electronic systems:

* rupture of thin films...

...stress, and

* intense electric fields that can cause interference or failure of nearby electronics.

The **ESD** susceptibilities of devices vary depending on their technology. The range of **ESD** threshold varies from 10 to 100V for MOSFETs, 300 to 7000V for bipolar devices, and...

...for CMOS devices. You need to select the appropriate device technology for the end application.

ESD prevention should occur at all stages--from manufacturing to the field. Some of the techniques that you can use to mitigate **ESD** problems in electronic circuits include using protective devices at critical points in the circuit; minimizing...

...good pc-board design; selecting components using the right technology with a higher level of **ESD** immunity; and shielding the circuit against **electrostatic** fields. You can use several models of **ESD** to simulate the effects of **ESD** on electronic components and specify thresholds for **ESD** immunity based on end-use requirements. The **ESD** models include the human-body model, the charged-device model, the machine model, and the...

...use the following circuit-design techniques:

* Choose components with a high level of immunity to **ESD** and EMI, with considerations for technology, speed, power requirements of your design, bandwidth, rise and...component mounted on it.

* Provide a transient-suppressor device and an inrush-current limiter for **ESD** -sensitive devices and at critical points in the circuit.

* To suppress noise, slip a ferrite...

...to critical components is to mount the transformer away from sensitive

components. Provision of an **electrostatic** shield between primary and secondary windings can reduce EMI. This shield is a thin copper...

...edges of the board and connecting this trace to ground can help to divert any **ESD** -induced discharge currents that result from human contact to ground. All the precautions you take during production and packing of **ESD** -sensitive components are pointless if operators carelessly handle and assemble boards. For this **ESD** problem, you can provide a guard trace by diverting the energy to ground. Provide a...

...electronic system. The principle of shielding is to absorb or reflect the incident electromagnetic or **electrostatic** field. At low frequencies, absorption of the incident magnetic field is the best method to...as a slot antenna. Unused connectors can charge, so you should keep them covered with **static** -dissipative material when you are not using them. All insulating parts in the cabinet should...

...shields should connect to a 360 (degrees) contact with the cabinet to avoid antenna effects.

Plastic materials coated with chemicals such as ammonium salts and amidoamines are available for packing sensitive **electronic components** . **ESD** control through **antistatic** flooring is a useful measure. **Containers** for storing sensitive components are available in the form of conductive **plastic** bins, **trays** , **tubes** , carbon-filled **plastics** , and metal-foil-lined **bags** . These **bags** can be single or multilayered, transparent, or opaque. The opaque **bags** are made of carbon-filled **plastic** and are inexpensive and rugged, which makes them sufficient for most **ESD** -control applications. Metallized- **plastic bags** , which are also transparent and moisture- and heat-resistant, are durable for storing assembled pc...

...and instrument panels. These I/O-shielding materials offer cost-effective shielding against EMI and **ESD** . Sources of electric charge in a production set-up include personnel, clothing, computer terminals, synthetic...

...coverings. Monitoring the handling of components, storage, assembly, testing, and other operations can help prevent **ESD** -induced damage to electronic devices. Conductive foams, **static** -dissipative bags, component storage bins, and tubes are also available for storing sensitive components. Place assembled pc boards in **static** -dissipative bags during storage and shipment. Such containers have a special coating to achieve surface...

...accumulation and potential differences between the pins of the device, which can also lead to **ESD** damage.

PREVENT THERMAL-OVERSTRESS FAILURES

Heat is one of the stress factors that affects all...

...dependent. Some of the common reasons for thermal overstress in a device are EOS and **ESD** . Thermal overstress causes damage, such as charring, melting of bond wires, and carbonation of the **plastic** encapsulating material. To prevent such failures, you need to operate a device within its SOA and provide adequate design safeguards against **ESD** , EMI, and thermal overstress. Thermal overstress causes thermal fatigue, thermal runaway, hot spots, and other...physical

changes

High-temperature burn-in	Surface and metallization faults, wire-bond defects

Humidity test	**Moisture absorption** , corrosion, chemical reaction
Salt spray	Resistance to corrosion, simulates coastal climate
Moisture resistance	Resistance to...

...die cracks, mismatches in the thermal coefficients of expansion, seal defects, and defects in the **plastic packages** .

Storage at high temperature subjects a component to a higher temperature than in burn-in...

...power or stimuli to the component. The test temperature is around 150 (degrees) C for **plastic** -encapsulated devices and 250 (degrees) C for hermetically sealed devices. Temperature exposure lasts 24 hours...field operation of equipment differ from lab conditions. Components may experience stresses, such as EMI, **ESD** transients, high temperature, corrosive chemical atmosphere, and vibration. Designers often derate the components in terms...

...a high degree of reliability.

TABLE A--DERATING GUIDELINES

Component	Type	Parameter	Derating factor
Capacitors	**Plastic** dielectric	Voltage rating	0.75
	Ceramic		0.75
	Tantalum electrolytic		0.6
	(solid)	temperature	0.4...0
ICs	Digital	Supply voltage	Within SOA limits
		Junction temperature	100 (degrees) C for **plastic**
			110 (degrees) C for hermetic
		Speed	0.75
		Input voltage	Within SOA limits
		Output current	0.8
	Analog	Supply voltage	Within SOA limits
		Junction temperature	100 (degrees) C for **plastic**

			110 (degrees) C for hermetic
		Input voltage	0.75
		Output voltage	0.8
		Power dissipation	0.75
Component	Type	Parameter	Comments
Capacitors	**Plastic** dielectric	Voltage rating	
	Ceramic		
	Tantalum electrolytic		If effective circuit impedance is > 3 (Omega)/V

(solid...
...the entire board to fail. Workers should be trained to carefully handle components by observing **ESD** and handling precautions during all stages of production.

EOS DESIGN FAULT

This bipolar-junction transistor...

...4.) Pollino, E, Microelectronic Reliability, Volume II, Artech House, Norwood, MA, 1981.

(5.) Boxleitner, Warren, **Electrostatic** Discharge and Electronic Equipment, IEEE Press, New York 1989.

(6.) Lakshminarayanan, V, "Revisiting environmental stress...

...successful EMC design," RE Design, September 1999, pgs 35 to 47.

(9.) Lakshminarayanan, V, "Minimize **ESD** -induced failures," Advanced Packaging, August 1999, pgs 36 to 39.

(10.) Bipolar Power Transistor Databook...

20000803

29/5,K/9 (Item 5 from file: 148)

07806380 SUPPLIER NUMBER: 17001020 (USE FORMAT 7 OR 9 FOR FULL TEXT)

Electronics firms wrap up success. (packaging of electronic components to be shipped by air freight) (Cover Story)

Thuermer, Karen
Air Cargo World, v85, n4, p24(5)
April, 1995
DOCUMENT TYPE: Cover Story ISSN: 0745-5100 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 1844 LINE COUNT: 00143

SPECIAL FEATURES: illustration; photograph

INDUSTRY CODES/NAMES: AERO Aerospace and Defense; TRAN Transportation, Distribution and Purchasing
DESCRIPTORS: Electronic components industry--Packaging; Air freight--Safety and security measures; Packaging--Management
PRODUCT/INDUSTRY NAMES: 3670000 (Electronic Components); 4502000 (Air Cargo Service)
SIC CODES: 3670 Electronic Components and Accessories; 4512 Air transportation, scheduled
FILE SEGMENT: TI File 148
... a sponge. For that reason, Adaptec no longer uses single tarps or foam inside the **packages** . "We replaced it with **plastic** anti- **static** **bags** when we started sterilizing our products," she said.
Monica Silvers, international transportation coordinator for Apple...

...To prevent moisture problems, Apple wraps its products in what she described as "old fashion **plastic** **bags** ." Inside the **packages** , they also use chaplets that draw the moisture away from the product.
Sometimes even the slightest moisture can damage **electronic** **components** , particularly **surface** **mounted** **devices** (**SMD**). Manufacturers and **packagers** of these products have reported increased product protection from humidity damage by using **Dry** **Pack** packaging manufactured by United **Desiccants** .
The small **moisture - adsorbing** **desiccants** packets seal moisture out, whereas the **humidity** **indicator** cards lets users know when the atmosphere around the electrical device reaches 10, 20, 30 and 40 percent relative humidity. The **humidity** **indicators** also allow each **package** to be visually inspected, to insure that the **SMD** is dry and ready for soldering without decohesion of the **plastic** from the underside of the leadframe die pad.
David Olsson, operations manager for William Wetmore...says. "My advice is to minimize the size within the technical constraints," such as electro **static** discharge and shock vibration protection.
Olsson recommends keeping the package to 64 inches or less...

19950400

29/5,K/11 (Item 7 from file: 148)

07607126 SUPPLIER NUMBER: 16528996 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Motorola deflates device damage.
Packaging Digest, v31, n12, p74(3)
Nov, 1994
ISSN: 0030-9117 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1866 LINE COUNT: 00147

ABSTRACT: Tempe, AZ-based Motorola encountered damage problems in shipping integrated circuit (IC) chip products for its Commercial Plus Technologies Operation. The firm's ICs were becoming more complicated that traditional packaging inevitably failed to protect the highly-sensitive products. Motorola found the solution in a joint venture project with Air Packaging Technologies. The joint effort generated the **Static** Discharge Shielding Air Box Reusable, an inflatable bag that protects and immobilizes the chips in an air cushion.

SPECIAL FEATURES: illustration; photograph
COMPANY NAMES: Motorola Inc.--Packaging; Air Packaging Technologies Inc. --Products

INDUSTRY CODES/NAMES: CONT Containers and Packaging
DESCRIPTORS: Semiconductor industry--Packaging; Packaging industry--Products
PRODUCT/INDUSTRY NAMES: 3674126 (IC Memory Chips); 2643900 (Bags NEC)
SIC CODES: 3674 Semiconductors and related devices; 2670 Misc. Converted Paper Products
FILE SEGMENT: TI File 148

...ABSTRACT: solution in a joint venture project with Air Packaging Technologies. The joint effort generated the **Static** Discharge Shielding Air Box Reusable, an inflatable bag that protects and immobilizes the chips in...

TEXT:

Reusable air **bag** for expensive **integrated circuits** offers improved protection from shock, **ESD** damage and moisture, cutting materials and labor costs 44 percent. Inflatable nylon/LLDPE bags replace ...

... joint venture effort by both Motorola and the bag's manufacturer, Air Packaging Technologies. Called **Static** Discharge Shielding (SDS) Air Box [R] Reusable, the bag has been used in CPTO's...

...see-through film of the air bag permits instant verification of contents and allows the **humidity indicator** card to be read without opening the package. Bar codes can also be scanned right...

...by 90 percent. Extensive drop tests show that cushion protection exceeds ISTA and ASTM standards.

* **ESD** protection exceeds current standards, according to several tests conducted by independent testing firms.

* High moisture...

...with the exception of an open end in which product is inserted along with a **humidity indicator** card from Humidial/United **Desiccants** . An operator applies pressurized air from an inexpensive regulator, supplied by Air Packaging Technologies, to...

...air gap/film/product/ film/air gap/film, is what gives the package its strong **ESD** protection. The air gaps can range anywhere from 1/2 to 1 in. thick, depending on the contents, and the **static** -dissipative bag material relies on nylon to give it a variety of performance characteristics. After ...

...Associates confirmed the combination of the material and the air gaps "provide a very good **ESD** package for essentially all devices under essentially all conditions." In one test, the **package** withstood a 20 kV discharge while containing **integrated circuits** that are rated at 150 v maximum.

In addition to providing cushioning capability and **ESD** protection, the air gap forms a strong moisture barrier. **Desiccant** pouches from Multiform **Desiccants** are also added to the air gap portion of the bag during bag manufacture to...

...either dry air or nitrogen which further restricts moisture vapor transmission and also contributes to **ESD** protection. Moisture barrier tests show a **desiccated** Air Box inflated with dry air to have a moisture vapor transmission rate of 0...

...24 hr at 100 percent relative humidity and 23 deg C.

Before ICs can be **packaged** , they are first placed in an **IC**

carrier , which can take one of three forms-- **plastic** **trays** , reels or rails, all from multiple suppliers, depending on the type of chip and customer...less complex and more rugged, although these chips too will eventually go in the air **bag** .

In the old packaging process, **IC** **carriers** were first stacked, strapped with **plastic** strapping material and wrapped in **antistatic** shrink film, from various suppliers. The shrink pack was then placed in metallized barrier bags along with **desiccant** pouches and a **humidity** **indicator** card. After being vacuum-sealed (which, Duncan points out, makes it difficult for **desiccants** to do their job well), the bags would be placed inside a primary corrugated container...

...sixth empty one for top protection) and placed in .029 paperboard end caps--instead of **plastic** strapping--from Arizona Paper Box and printed in soybean ink with the Motorola logo, an **ESD** warning, and a recycled logo. The end caps, which are hand-formed immediately prior to application, are easier to apply and remove, and are being recycled, which the **plastic** straps weren't. Bar code labels are placed on the end caps with a part...

...as a listing of the standards that the bag passes. Information currently applied by the **static** treatment coater but which in the future will be preprinted includes a date code for **static** -dissipative treatment and international symbols indicating **ESD** and moisture sensitivity.

At the point of use in the customer's plant, bags are...
...air escapes. The bag's sealed edge is trimmed off, and the operator removes the **IC** **carriers** . Although Motorola is not currently doing so, it plans to rouse the bags at least...

...is available: Air Box--Air Packaging Technologies, Inc., 25620 Rye Canyon Rd., Valencia, Calif. 91355.

Humidity **indicator** card--Humidial/United **Desiccants** , Box 610, Colton, Calif. 92324.

Desiccant pouch--Multiform **Desiccants** , Inc., 960 Busti-at-Niagara, Buffalo, N.Y. 14213.

Paperboard end caps--Arizona Paper Box, P.O. Drawer 1219, Spring Valley, Calif. 91977.

ESD testing--Fowler Associates, Inc., 3551 Moore-Duncan Hwy., Moore, S.C. 29369.

Biax nylon rollstock...

...Packaging, 285 Industrial Pkwy. S., Aurora, Ont. L4G 3V8. Canada.

Inner film LLDPE resin--Dow **Plastics** , 2040 Dow Center, Box 1206, Midland, Mich. 48674.

AmeriStar competition--Institute of Packaging Professionals, 481...

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					Aug 05, 2001	Aug 05, 2002	
					Dec 10, 2001	Nov 21, 2002	
						Dec 05, 2002	

Home | Help

TECHNICAL GLOSSARY

From A to Z, we created a vast list of Glossary terms to assist you. We have given you two ways to search you can either go directly to the term, using the drop down list or you can scroll through the entire glossary.

Find it! Submit

XMS-EXTENDED MEMORY SPECIFICATION Get the Definiton

We have listed our entire glossary below for easy navigation.

(AGP)-ACCELERATED GRAPHICS PORT
High speed graphics. Data shifts directly from the graphics controller and the computer memory, bypassing the cache in video memory.

ACCESS TIME
The average time period, for RAM, between a query for information and its completed access.

AMRAY
Equipment used to gauge crucial information from an area on a semiconductor component at various levels of operations through the use of a Scanning Electron Microscope(SEM).

ANSI-(AMERICAN NATIONAL STANDARDS INSTITUTE)
The United States organization responsible for setting information technology standards.

ARRAY
This is a large rectangular area in the center of a semiconductor component where memory is stored. Memory is stored in cells at each intersection of columns and rows, each of which holds a bit.

ASCII(American Standard Code for Information Interchange)
A method of encoding text as binary values. The ASCII system requires nearly 256 combinations of 8-bit binary numbers to support every possible keystroke from the keyboard.

ASIC-(APPLICATION-SPECIFIC INTEGRATED CIRCUIT)
These chips are created for a specific application rather than common use. Integrated-circuit chips are typically used in video boards and modems.

ASYNCHRONOUS
A process involving numerous tasks being performed independently in a system.

ATA-(AT ATTACHMENT)
A specification that integrates the drive control electronics interface. AT refers to the IBM PC/AT personal computer and its bus architecture.

AUTO PRECHARGE

A DRAM feature that enables the circuitry in a memory chip to automatically close a page at the end of a request from the processor for a single block of data.

BACKSIDE BUS(BSB)
BSB is the path in which data flows between the computer processing unit and the level 2 cache.

Bandwidth
The capacity to move data on an electronic line such as a bus or a channel. In short, the amount of data moved relative to a specific time frame. It is expressed in bits, bytes, or Hertz (cycles) per second.

Bank (l gical memory bank)
A collection of memory slots in a computer which work together as a single unit. A bank cannot be partially filled and must be filled with like modules (same size, speed and type).

BANK SCHEMA
A procedure in which memory configuration is diagramed. Independent sockets are represented by rows and banks are illustrated by columns.

BASE RAMBUS
The beginning of Rambus technology, shipped first in 1995.

BEDO-(BURST EDO)
Similar to EDO DRAM, Burst EDO cycles are assembled in bursts of four. Bus speeds of Burst EDO range from 40mhz to FPM or EDO DRAM.

Binary
A method of encoding numbers as a series of bits. The binary number system, also referred to as base 2, uses combinations of only two digits- 1 and 0.

BIOS-(BASIC INPUT/OUTPUT SYSTEM
A set of low level RAMBUS that allow a computer's application programs and operating systems to read characters from the keyboard, output characters to printers, and interact with the hardware in other ways.

Bit
A binary digit- the smallest unit of information a computer system can process. It can have a value of only 1 or 0 (off or on). Single bits are too small to be of much use and are usually classified in groups such as bytes of binary words.

BLOCK
A block is a physical unit of data in a logical record that is expressed in bytes.

BLOCK DIAGRAM
A diagram of the system dealing with important functions and interconnections between them.

Brand- n-Brand Memory
(See original memory).

BUFFER
Shared information from devices operating at different speeds are held in the buffer. This buffer enables a device to function without delays from other mechanisms.

BUFFERED MEMORY
A module that houses buffers, which are used to help control the signals the memory chips receive. In addition, they allow the module to include more memory chips. Buffered and non-buffered memory cannot be combined.

BURN-IN
Using a high voltage and temperature to test an integrated circuit. This procedure will find those chips that tend to fail early during actual use. Chips that pass tend to have a

longer life expectancy than required for regular use.

BURST EDO RAM
EDO Memory that processes four memory addresses in one burst. Speeds of the Bus may range from 50mhz to 66mhz.

BURST MODE
A high speed transmission of a series of addresses that occur when the processor asks for a single address.

Bus
The central communication avenue in a PCs system board. If normally consists of a set of parallel wires or signal traces that connect the CPU, the memory, all input/output devices, and peripherals.

Bus cycle
A single transaction between system memory and the CPU.

Byte
A unit of information made up of 8 bits. The byte is the key component of computer processing; most computer component specifications are measured in bytes or multiples thereof (such as kilobytes or megabytes).

Cache
A type of memory which is used to store frequently used instructions and data. Cache memories are used to increase the performance of computing systems by holding these frequently used instructions and data closer (in a speed-related context) to their final destination.

CAPACITANCE
The characteristic of a circuit element that enables it to store an electrical charge.

CAS LATENCY
The ratio between column access time and clock cycle time.

CAS-(COLUMN ADDRESS STROBE)
A memory chip signal that connects the column address of a specific location in a row-column configuration.

CE
The international symbol on all electrical equipment stating that it was certified per EN50082-2 (immunity) and EM5501A (emissions).

CHECK BITS
Additional data bits that a module supplies to support ECC.

CHIP-SCALE PACKAGE
Thin chip package in which electrical connections are usually through a ball grid array. Used in RDRAM and flash memory.

CHIPSET
The computer processing unit is supported by the chipset, a set of microchips which contain several controllers, determining how data travels between components and the processor.

CHMOS
Complementary High-density Metal Oxide Semiconductor,

CISC-(COMPLEX INSTRUCTION SET COMPUTING
A design logic in which chips combine multi-step instructions into one command. CISC is usually associated with microprocessors.

CLOCK RATE
The number of pulses discharged by a computer's clock in a one second interval. In a synchronous computer, clock rate establishes the time period in which logical or arithmetic gating occurs.

COB-(CHIP ON BOARD)
A technique or system in which semiconductor dice are connected to a PC board with bonded wires or solder balls.

COLUMN
A portion of the memory array whereby information is stored at the junction of a column and a row.

COMPACT FLASH
Removable storage cards that are efficient in terms of weight, size, and durability. In addition, they utilize small amounts of voltage and retain information when the power is off. Often used in digital cameras, printers, and handheld computers.

Comp site Memory
A term used by Apple Computer to describe modules which use many low-density memory (4 Megabit) chips.

CONCURRENT RAMBUS
The second generation of Rambus technology.

CONTROLLER
A major component of a computer that interprets and performs program commands.

COPLANARITY
In terms of a semiconductor package, coplanarity refers to the condition of leads between two parallel planes.

CPU
Central Processing Unit. The "brains" of a computer system. A CPU is an integrated circuit which processes the bulk of the data and software instructions in a computer system. It is commonly referred to as "the processor" in a computer system.

CRC-(CYCLICAL REDUNDANCY CHECK
A mathematical method to discover errors involving long runs of information with a greater degree of accuracy.

Credit Card Memory
A type of memory module (much like a PCMCIA card) named for its size. Credit card modules are commonly used in notebooks and other portable computing devices.

CRIMM-(CONTINUITY RIMM)
Direct Rambus memory in which the module does not contain any memory chips. Used to fill unused RIMM sockets to allow for an uninterrupted pathway for a signal.

DAMPING
The deterioration of oscillations as a result of the resistance in resonant circuits.

DATA OUT
The pathway that transmits the information from the RAM.

DATE CODE
A mark placed on PCBs and DRAM indicating the date that the product was manufactured.

DDR (Double Data Rate) r SDRAM II
The next generation of SDRAM. DDR is based on the same design as SDRAM, but its speed capabilities are enhanced. DDR allows data to be read on both the rising and the falling edge of the clock cycle, delivering twice the bandwidth of standard SDRAMs. DDR, in effect, doubles memory speed without increasing the clock frequency.

DIE
Die refers to one unpackaged part of thousands of tiny electronic parts forming the internal circuitry of a semiconductor component. It is also known as an integrated circuit or chip.

DIE PICK-UP TOOL
The tool on the machine that picks up the semiconductor component or part and places it on the leadframe.

DIE SIZE
Die size is the physical measurements of the die.

DIELECTRIC
Components used in semiconductor processing that, when voltage is applied, conduct no current. Examples of dielectrics include silicon dioxide and silicon nitride.

DIELECTRIC DEPOSITION
When a layer of deposited oxide is applied to separate (isolate) two metals in a double-level metal process. Must be accomplished in a way that prevents hillock formation on the top level.

DIMM
Dual In-Line Memory Module. A type of memory with contacts along one edge of a printed circuit board. A DIMM is much like a SIMM except the contacts on either side of a DIMM are not electrically connected like they are on a SIMM (pin 1 on the back and pin 1 on the front do not make the same connection). See also: memory module, SIMM.

DIP (Dual In-line Package)
A form of DRAM component packaging. DIPS are installed either in sockets or permanently soldered into a hole extending into the surface of the printed circuit board.

DIRECT ADDRESS
A memory address contained as part of the instruction.

DIRECT MEMORY ACCESS
A computer characteristic that enables peripheral systems to access memory for read and write operations, yet not affect the central processor of a computer.

DIRECT RAMBUS
Rambus technology's third generation, which offers a completely new DRAM architecture for high-performance PCs.

DISTRIBUTED PROCESSING
A process which frees the CPU of the details of block transfers by utilizing intelligent input/output controllers and direct memory access.

DRAM
Dynamic Random Access Memory. The most common form of primary storage used in computer systems. This type of memory must be 'refreshed' periodically to maintain the stored data (hence the term dynamic). The data in DRAM is lost when the power is removed from the circuit: therefore, the data in DRAM must be moved to a secondary storage device such as a hard drive floppy drive.

DRIVER BOARD
A PCB that transmits signals between the interface board of the oven and the DUT board. For each oven slot, there is a corresponding driver board situated in the rear of the oven.

DRY PACK

A method for preparing product to be shipped. It involves placing product, a clay desiccant, and an HIC (humidity indicator card) into a vacuum-sealed moisture vapor barrier bag.

INTERNET ARCHIVE
WaybackMachine

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Searched for **http://www.intel.com/design/quality/icstorage/env_short_term.htm**

4 Results

* denotes when site was updated.

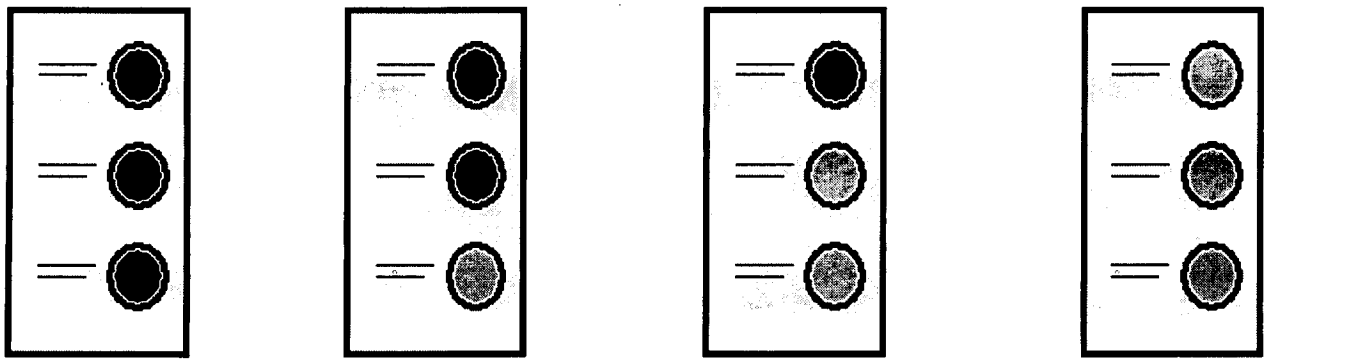
Search Results for Jan 01, 1996 - Dec 01, 2003

1996	1997	1998	1999	2000	2001	2002	2003
0 pages	0 pages	0 pages	0 pages	0 pages	1 pages	3 pages	0 pages
					Jul 14, 2001 *	Jan 04, 2002 * Mar 11, 2002 Oct 31, 2002 *	

Integrated Circuit (IC) Storage and Handling: Damage Prevention

General Device Storage: Safe Environmental Conditions: *Short term*

- Short-term storage:
  - Short term storage is considered to be up to 1 year.
  - Customers need to follow established handling/storage practices so as to ensure reliable manufacture of their product.
- Moisture related failures:
  - Affected devices are packed in Moisture Barrier Bags (MBBs) with a desiccant and Humidity Indicator Card (HIC).
  - Packaging guarantees a minimum shelf life of 12 months at 40°C/90% relative humidity (RH), provided that bag integrity is not violated.
  - After the 12 month period has expired, the user must examine the HIC to see if the moisture content is low enough for safe usage.
  - If HIC indicates that the allowable moisture level has been exceeded, then devices must be baked to remove excess moisture prior to the soldering process.
  - For more information, see device moisture sensitivities.



- A pre-solder bake will be required if:
  - MBBs are damaged during short term storage.
  - Devices are NOT soldered within the time stipulated on MBB label.
  - Devices have been stored for many years and desiccant has expired.
- Conditions for bake:
  - Low Temperature Bake:
    - 192 hours at 40°C +5°C/-0°C and <5% relative humidity (RH)
    - Standard bake which guarantees stability of tube/tape and reel dimensions
  - High Temperature Bake:
    - 24 hours at 125°C +/-5°C
    - For devices out of packaging or devices supplied in high temperature trays

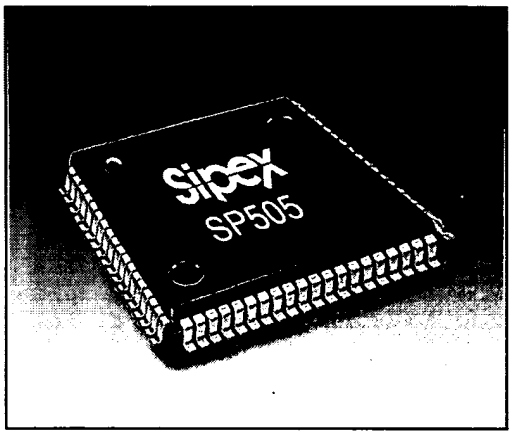
back

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP505

WAN Multi-Mode Serial Transceiver

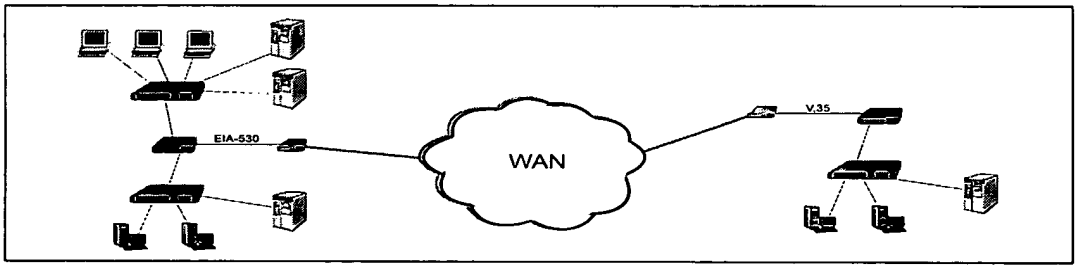
- +5V Only Operation
- Seven (7) Drivers and Seven (7) Receivers
- Driver and Receiver Tri-state Control
- Internal Transceiver Termination Resistors for V.11 and V.35 Protocols
- Loopback Self-Test Mode
- Software Selectable Protocol Selection
- Interface Modes Supported:
  - ✓ RS-232 (V.28)
  - ✓ X.21/RS-422 (V.11)
  - ✓ EIA-530 (V.10 & V.11)
  - ✓ EIA-530A (V.10 & V.11)
  - ✓ RS-449 (V.10 & V.11)
  - ✓ V.35 (V.35 & V.28)
  - ✓ V.36 (V.10 & V.11)
  - ✓ RS-485 (un-terminated V.11)
- Improved ESD Tolerance for Analog I/Os
- High Differential Transmission Rates
  - ➥ SP505A - 10Mbps
  - ➥ SP505B - over 16Mbps
- Compliant to NET1/2 and TBR2 Physical Layer Requirements
  (TUV Test Report NET2/052101/98)
  (TUV Test Report CTR2/052101/98)



DESCRIPTION...

The **SP505** is a monolithic device that supports eight (8) popular serial interface standards for DTE to DCE connectivity. The **SP505** is fabricated using a low power BiCMOS process technology, and incorporates a Sipex patented (5,306,954) charge pump allowing +5V only operation. Seven (7) drivers and seven (7) receivers can be configured via software for any of the above interface modes at any time. The **SP505** requires no additional external components for compliant operation for all of the eight (8) modes of operation. All necessary termination is integrated within the **SP505** and is switchable when V.35 drivers, V.35 receivers, and V.11 receivers are used. The **SP505** can operate as either a DTE or DCE.

Additional features with the **SP505** include internal loopback that can be initiated in either single-ended or differential modes. While in loopback mode, driver outputs are internally connected to receiver inputs creating an internal signal path convenient for diagnostic testing. This eliminates the need for an external loopback plug. The **SP505** also includes a latch enable pin with the driver and receiver address decoder. Tri-state ability for the driver and receiver outputs is controlled by supplying a 4-bit word into the address decoder. Seven (7) drivers and one (1) receiver in the **SP505** include separate enable pins for added convenience. The **SP505** is ideal for WAN serial ports in networking equipment such as routers, switches, DSU/CSU's, and other access devices.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +7V
Input Voltages:
- Logic ..... -0.3V to (V_{CC}+0.5V)
- Drivers ..... -0.3V to (V_{CC}+0.5V)
- Receivers ..... ±15.5V

Output Voltages:
- Logic ..... -0.3V to (V_{CC}+0.5V)
- Drivers ..... ±15V
- Receivers ..... -0.3V to (V_{CC}+0.5V)

Storage Temperature ..... -65°C to +150°C
Power Dissipation 2000mW
Package Derating:
- $ø_{JA}$ ..... 46°C/W
- $ø_{JC}$ ..... 16°C/W

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 80-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order remove moisture prior to soldering. Sipex ships the 80-pin QFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT} = –3.2mA
V_{OH}	2.4			Volts	I_{OUT} = 1.0mA
V.28 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±15	Volts	per Figure 1
Loaded Voltage	±5.0		±15	Volts	per Figure 2
Short-Circuit Current			±100	mA	per Figure 4
Power-Off Impedance	300			Ω	per Figure 5
AC Parameters					**V_{CC} = +5V for AC parameters**
Outputs					
Transition Time			1.5	µs	per Figure 6; +3V to -3V
Instantaneous Slew Rate			30	V/µs	per Figure 3
Propagation Delay					
t_{PHL}	0.5	1	5	µs	
t_{PLH}	0.5	1	5	µs	
Max.Transmission Rate	120	230		kbps	
V.28 RECEIVER					
DC Parameters					
Inputs					
Input Impedance	3		7	kΩ	per Figure 7
Open-Circuit Bias			+2.0	Volts	per Figure 8
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
AC Parameters					**V_{CC} = +5V for AC parameters**
Propagation Delay					
t_{PHL}	50	100	500	ns	
t_{PLH}	50	100	500	ns	

⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　昭62－158042

⑤Int.Cl.⁴	識別記号	庁内整理番号	㊸公開　昭和62年(1987)7月14日
B 32 B 27/18 27/08		J－7112－4F 7112－4F	

審査請求　未請求　発明の数 1　（全3頁）

㊹発明の名称　ヒートシール容易な制電コートフイルム

㉑特　願　昭61－281

㉒出　願　昭61(1986)1月7日

㉒発明者　服部　英二　鈴鹿市平田中町1番1号　旭化成工業株式会社内

㉑出願人　旭化成工業株式会社　大阪市北区堂島浜1丁目2番6号

㉔代理人　弁理士　野崎　鎭也

明　細　書

1．発明の名称

ヒートシール容易な制電コートフイルム

2．特許請求の範囲

1　プラスチックフイルムのヒートシールできる面Aに、カーボンブラックを含み透視できる導電層Bと、ウレタンプレポリマー10～50％を含む二次転移温度90℃以下のアクリル樹脂層Cとを、Aに対しB、Cの順にコートして硬化した上記コート面でヒートシール容易な制電コートフイルム。

2　導電層Bがメッシユ状に塗布されている特許請求の範囲第一項記載の制電コートフイルム。

3．発明の詳細な説明

（産業上の利用分野）

本発明は静電気障害を受けやすい物品の包装に使用する制電コートフイルムに関するものであって、特に制電コート面でヒートシールして袋などの形状にして使用するのに適したフイルムに関する。

（従来の技術）

通常のプラスチックフイルムはその表面抵抗値（JIS K6911に準拠した測定値をいう。以下同じ）が$10^{14}\Omega$以上であり、フイルム自体も容易に帯電し、又、そのフイルムと接触し摩擦を受ける他の物体を強く帯電させるので、静電気障害を受け易い物品を包装するためには帯電防止処理することが必要であった。本発明者等は、先に表面抵抗が低く、かつ透視可能な帯電防止プラスチックフイルムを完成し出願した（特開昭60－214945号）。

更に、前記の帯電防止フイルムを用いて、静電気障害を受け易い物品の保護に最も適した包装体について研究を重ねた結果、表面抵抗が低い面が、包装体の外側ではなく、被包装物の側にあることが、被包装物保護のために特に有利であることを見出し、これにもとずき、静電気障害を受け易い物品の保護に有効な袋の構造についての発明を完成し、特願昭59－199975号を出願した。

しかし、表面抵抗が低いフイルム面を得るために、カーボンブラックを導電材料とする透視可能

DERWENT-ACC-NO: 1987-232702

DERWENT-WEEK: 198733

TITLE: Readily heat-sealable plastic film - having charge-controlling coating contg. carbon black, and acrylic! resin layer contg. urethane prepolymer

PATENT-ASSIGNEE: ASAHI CHEM IND CO LTD[ASAH]

PRIORITY-DATA: 1986JP-0000281 (January 7, 1986)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 62158042 A	July 14, 1987	N/A	003	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 62158042A	N/A	1986JP-0000281	January 7, 1986

INT-CL (IPC): B32B027/18

ABSTRACTED-PUB-NO: JP 62158042A

BASIC-ABSTRACT:

Film is composed of a plastic film having a heat sealable surface, an electroconductive layer contg. carbon black and capable of being seen through, and an acrylic resin layer contg. 10-50 % urethane prepolymer and having a sec. transition temp. below 90 deg.C. The layers are coated and cured in this order on the heat sealable surface of the plastic film. Specifically the electroconductive layer is a mesh-form coat.

Plastic film is polyethylene, EVA, polypropylene, 1,2-polybutadiene, etc. A polyester film coated with an ethylene-vinyl acetate copolymer is exemplified. A pref. urethane prepolymer is a two-liq. type consisting of a polyol and a polyisocyanate or a moisture-curable liquid type. A pref. electroconductive layer is formed of partially-saponified EVA copolymer contg. carbon black.

USE/ADVANTAGE - For packaging of articles which are liable to suffer electrostatic problems i.e. IC's. The film can be easily formed into a bag. The mesh-form electroconductive layer contributes to the high heat-sealing property. Contents of the bag can be seen.

CHOSEN-DRAWING: Dwg.0/0

TITLE-TERMS: READY HEAT SEAL PLASTIC FILM CHARGE CONTROL COATING CONTAIN CARBON BLACK POLYACRYLIC RESIN LAYER CONTAIN URETHANE PREPOLYMER

ADDL-INDEXING-TERMS:
POLYETHYLENE@ POLYVINYL ACETATE POLYPROPYLENE@ POLYBUTADIENE POLYESTER

DERWENT-CLASS: A14 A25 A85 A94 P73

CPI-CODES: A08-M09A; A08-R03; A09-A03; A10-E24; A12-P01A; A12-S06C;

UNLINKED-DERWENT-REGISTRY-NUMBERS: 5085U

POLYMER-MULTIPUNCH-CODES-AND-KEY-SERIALS:
Key Serials: 0218 0226 0231 0241 3155 0486 0487 0789 3185 1758 2007 2008 2020 2021 2022 2198 2217 2274 2278 2437 2493 2513 2551 2553 2595 3254 2667 2726 2743 2774 2776 0239 0248 1073 1093 1291
Multipunch Codes: 014 02& 034 04- 040 041 046 047 066 067 074 081 150 209 231 244 245 250 27& 307 308 310 318 321 326 359 373 381 431 435 443 473 477 50& 506 509 511 516 523 56& 58- 597 600 604 608 623 627 688 722 723 724 014 02& 034 04- 040 041 046 047 050 066 067 074 081 150 209 231 244 245 250 27& 307 308 310 318 321 326 359 373 381 431 435 443 473 477 50& 506 509 511 516 523 56& 58- 597 600 604 608 623 627 688 722 723 724 014 02& 034 04- 040 041 046 047 066 067 074 081 117 118 122 150 209 231 244 245 250 27& 307 308 310 318 321 326 359 373 381 431 435 443 473 477 50& 506 509 511 516 523 56& 58- 597 600 604 608 623 627 688 722 723 724 014 02& 034 04- 040 041 046 047 066 067 074 081 143 144 150 209 231 244 245 250 27& 307 308 310 318 321 326 359 373 381 431 435 443 473 477 50& 506 509 511 516 523 56& 58- 597 600 604 608 623 627 688 722 723 724

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1987-098374

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（A）　(11)特許出願公開番号

特開平4－367457

(43)公開日　平成４年(1992)12月18日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｂ６５Ｄ　73/02		Ｊ　7191－3Ｅ		
		Ｍ　7191－3Ｅ		

審査請求　未請求　請求項の数２(全　7　頁)

(21)出願番号　特願平3－155383

(22)出願日　平成３年(1991)５月31日

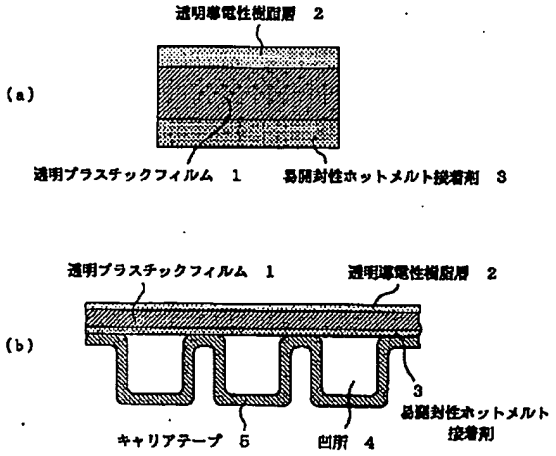
(71)出願人　000190116
信越ポリマー株式会社
東京都中央区日本橋本町４丁目３番５号
(72)発明者　林　修身
埼玉県大宮市吉野町１丁目406番地１　信越ポリマー株式会社商品研究所内
(74)代理人　弁理士　山本　亮一　(外１名)

(54)【発明の名称】　カバーテープフイルムおよびこれを使用した実装部品包装体

(57)【要約】　(修正有)

【目的】　高温高温下に長期間さらしても表面抵抗が上昇することなく、透明性に優れ、スティッキングを起こさず、長期間清掃する必要のない実装部品包装体を提供する。

【構成】　透明プラスチックフィルム１の表面に、平均粒径が０．３μｍ以下の酸化スズ化合物および／または酸化インジウム化合物の微粉末とバインダー樹脂とから成る透明導電性樹脂層２を設け、裏面にホットメルト接着剤層３を設けた透明性複合カバーテープフィルムと、帯電防止または導電性の樹脂シートに実装部品を収納する凹部４を連続的に設けたキャリアテープ５とよりなり、該ホットメルト接着剤層で該キャリアテープが易開封性に熱シールされている。



DERWENT-ACC-NO: 1993-041302

DERWENT-WEEK: 199305

TITLE: Cover tape film for package for mounting (e.g. electronic) parts - comprising hot melt adhesive backing, transparent plastic film and conductive layer of binder contg. tin oxide and/or indium oxide fine particles

PATENT-ASSIGNEE: SHINETSU POLYMER CO[SHPL]

PRIORITY-DATA: 1991JP-0155383 (May 31, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 04367457 A	December 18, 1992	N/A	004	B65D 073/02

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 04367457A	N/A	1991JP-0155383	May 31, 1991

INT-CL (IPC): B65D073/02

ABSTRACTED-PUB-NO: JP 04367457A

BASIC-ABSTRACT:

The cover tape film is formed as follows: (a) a transparent conductive resin film comprising tin oxide and/or indium oxide film fine powder with average grain dia. up to 0.3 microns and a binder resin is formed on the surface of a transparent plastic film; and (b) A hot melt adhesive layer is provided on the rear of the film. The mounting parts packaging body comprises; the cover tape film and a carrier tape with recesses for housing mounting parts in an antistatic or conductive resin sheet. The carrier tape is heat-sealed by the hot melt adhesive layer for easy opening.

USE/ADVANTAGE - The cover tape film is used for a mounting parts packaging body for housing various electronic parts, precision, or ICs. The packaging body has no increase in surface resistance even if the packaging body is continuously exposed to high temp. and high humidity. It is transparent, generates no sticking and requires no cleaning for a long period.

CHOSEN-DRAWING: Dwg.0/2

TITLE-TERMS: COVER TAPE FILM PACKAGE MOUNT ELECTRONIC PART COMPRISE HOT MELT ADHESIVE BACKING TRANSPARENT PLASTIC FILM CONDUCTING LAYER BIND CONTAIN TIN OXIDE INDIUM OXIDE FINE PARTICLE

DERWENT-CLASS: A92 Q34

CPI-CODES: A09-A02; A09-A03; A11-C01A; A11-C04B2; A12-E07C; A12-S06;

POLYMER-MULTIPUNCH-CODES-AND-KEY-SERIALS:
Key Serials: 0141 0150 0231 2211 2319 2426 2437 2513 2542 2551 2595 2600 2649 2651 2682 2684 2737 2740 2774 3253 3279
Multipunch Codes: 014 04- 08& 09- 15- 17& 308 331 342 381 393 431 435 443 479 506 509 516 523 541 55& 575 58& 592 593 597 600 609 623 627 628 725 014 04- 331 36& 381 431 443 506 509 516 523 541 55& 58& 597 600 609 623 627 628

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C1993-018728
Non-CPI Secondary Accession Numbers: N1993-031740

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号

特開平5－311061

(43)公開日　平成５年(1993)11月22日

(51)Int.Cl.[5]		識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｃ０８Ｌ	69/00	ＬＰＰ	8416－4Ｊ		
Ｃ０８Ｋ	3/04	ＫＫＨ	7242－4Ｊ		
//Ｈ０１Ｂ	1/24	Ｚ	7244－5Ｇ		
（Ｃ０８Ｌ	69/00				
	23:08）				

審査請求　未請求　請求項の数２(全　６　頁)

(21)出願番号　特願平4－142001

(22)出願日　平成４年(1992)５月８日

(71)出願人　000003296
電気化学工業株式会社
東京都千代田区有楽町１丁目４番１号

(72)発明者　木村　知弘
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(72)発明者　横山　聡
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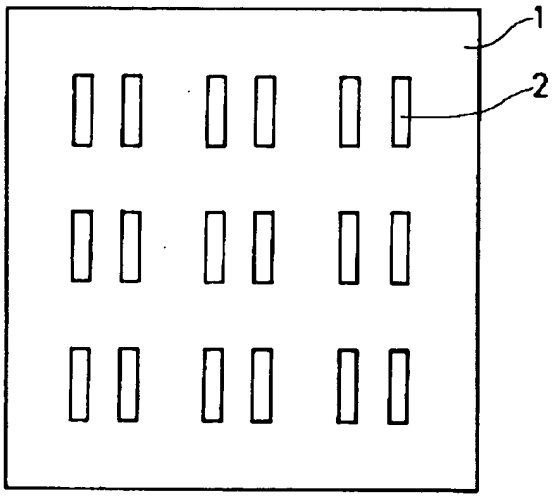
(72)発明者　鍋田　健司
東京都町田市旭町３丁目５番１号　電気化学工業株式会社総合研究所内

(54)【発明の名称】　耐熱導電性樹脂組成物及びその成形品

(57)【要約】

【目的】　耐熱導電性樹脂組成物として、制電特性、機械的物性及び高温加熱下での寸法安定性に優れ、また卓越した衝撃強度を有する帯電・静電気防止用の成形品に利用できる樹脂組成のものを得る。

【構成】　ポリカーボネート樹脂１００重量部、カーボンブラック１０～４５重量部及びエチレン－アクリル酸エステル共重合体１～２０重量部からなる樹脂組成物。



DERWENT-ACC-NO: 1993-411035

DERWENT-WEEK: 199351

TITLE: Heat resistant electroconductive resin compsn. for moulded prod. - contains polycarbonate resin, carbon@ black and ethylene@!-acrylic!-ester ! copolymer resin

PATENT-ASSIGNEE: DENKI KAGAKU KOGYO KK[ELED]

PRIORITY-DATA: 1992JP-0142001 (May 8, 1992)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 05311061 A	November 22, 1993	N/A	006	C08L 069/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 05311061A	N/A	1992JP-0142001	May 8, 1992

INT-CL (IPC): C08K003/04, C08L069/00 , H01B001/24 , C08L023:08 , C08L069/00

ABSTRACTED-PUB-NO: JP 05311061A

BASIC-ABSTRACT:

The resin compsn. contains 100 pts. wt. of (A) polycarbonate resin, 10 to 45 pts. wt. of (B) C black and 1 to 20 pts. wt. of (C) ethylene-acrylic ester copolymer resin as reinforcing material.

(A) has a viscosity average mol.wt. of 10,000 to 50,000, pref. 25,000 to 30,000. (B) has a particle dia. of 10 to 300 microns, a DBP absorption of 300 to 500 cc/100 mg. and has a specific surface area of 20 to 1,800 g/m2, and is pref. furnace black. Pref. (C) is ethylene-ethyl acrylate copolymer resin having an ethyl acrylate content of 10 to 50 mol. %. The resin compsn. may contain antioxidant and lubricant in 1 to 10 and 0.1 to 10 pts. wt. respectively per 100 pts. wt. of (A).

ADVANTAGE - The resin compsn. has excellent antistatic and mechanical properties, high dimensional stability under heating at elevated temp. and high impact strength. It is useful for antistatic moulded prod. such as plastic tray for transport, storage and drying of semiconductor integrated circuit device.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: HEAT RESISTANCE ELECTROCONDUCTING RESIN COMPOSITION MOULD PRODUCT CONTAIN POLYCARBONATE RESIN CARBON@ BLACK POLYETHYLENE@ POLYACRYLIC POLYESTER COPOLYMER RESIN

DERWENT-CLASS: A23 A85 L03 U11 X12 X25

CPI-CODES: A04-F06B; A04-G08A; A05-E06A; A08-R03; A08-R08; A09-A01A; A09-A03; A12-S08E; L03-A02E; L04-D10;

EPI-CODES: U11-A07; X12-D01X; X25-S;

UNLINKED-DERWENT-REGISTRY-NUMBERS: 5085U

ENHANCED-POLYMER-INDEXING:
Polymer Index [1.1]
017 ; H0022 H0011 ; R00326 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D82 ; G0340*R G0339 G0260 G0022 D01 D12 D10 D51 D53 D58 D63 F41 ; S9999 S1434 ; A999 A782 ; A999 A419 ; P1150 ; P0088
Polymer Index [1.2]
017 ; H0022 H0011 ; R00326 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D82 ; R01126 G0340 G0339 G0260 G0022 D01 D11 D10 D12 D51 D53 D58 D63 D85 F41 ; S9999 S1434 ; A999 A782 ; A999 A419 ; P1150 ; P0088 ; P0180
Polymer Index [1.3]
017 ; ND04 ; K9745*R ; B9999 B3305 B3292 B3190 ; B9999 B3747*R ; B9999 B3758*R B3747 ; B9999 B4159 B4091 B3838 B3747 ; Q9999 Q8571 Q8366 ; Q9999 Q7476 Q7330 ; K9461 ; B9999 B3178 ; B9999 B4682 B4568
Polymer Index [1.4]
017 ; A999 A497 A486 ; A999 A340*R
Polymer Index [1.5]
017 ; R05085 D00 D09 C* 4A ; A999 A237 ; A999 A760 ; S9999 S1456*R

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平6－350021

(43)公開日　平成６年(1994)12月22日

(51)Int.Cl.[5]		識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ	25/00	Ｂ			
	23/50	Ｘ			
	23/60				
				Ｈ０１Ｌ　23/ 56	Ｂ

審査請求　未請求　請求項の数１　ＯＬ　（全 ３ 頁）

(21)出願番号　特願平5－140315

(22)出願日　平成５年(1993)６月11日

(71)出願人　000005108
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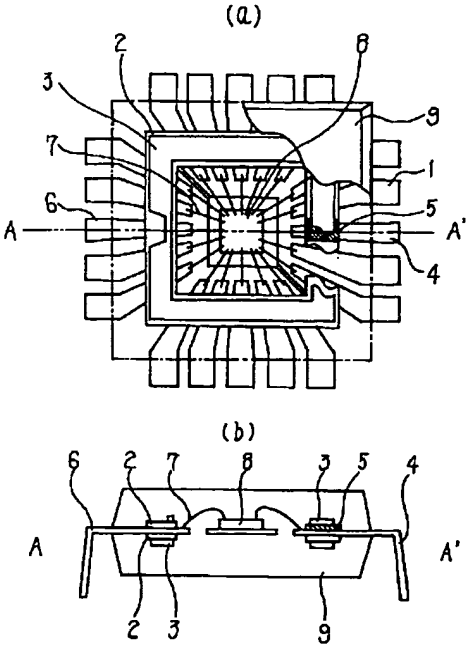
(74)代理人　弁理士　小川　勝男

最終頁に続く

(54)【発明の名称】　リードフレーム

(57)【要約】
【目的】半導体装置用のリードフレームにおいて、リードフレームと電源の間に容量を持たせ、このリードフレームを用いることによってＩＣの静電耐圧を向上させることが目的である。
【構成】４２合金等でできたリードフレームの本体１の上に絶縁物の薄膜２、さらにその上に導体３をおきこの絶縁物の薄膜を任意のリード上では、導体とすることによって、そのリードと絶縁物上の導体を接続する。
【効果】本発明によってＩＣの静電耐圧向上を行うことが簡便になる。またリードフレームを両側から導体ではさみ、その電位を異なる電源とした場合、電源間にも容量が付くため電源ノイズを低減することが出来る。

図１



DERWENT-ACC-NO: 1995-072033

DERWENT-WEEK: 199510

TITLE: Lead frame for plastic package type IC(s) - has lead over which thin film of insulator and conductor are deposited and connected to IC chip to improve electrostatic breakdown resistance

PATENT-ASSIGNEE: HITACHI LTD[HITA]

PRIORITY-DATA: 1993JP-0140315 (June 11, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 06350021 A	December 22, 1994	N/A	003	H01L 025/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 06350021A	N/A	1993JP-0140315	June 11, 1993

INT-CL (IPC): H01L023/50, H01L023/60 , H01L025/00

ABSTRACTED-PUB-NO: JP 06350021A

BASIC-ABSTRACT:

The lead frame has a main part (1) made of a metal alloy. A lead is connected to the IC chip (8). A thin film (2) of an insulator, is deposited on this lead. Another thin film (3) of an electric conductor is laid over this structure. The lead is then connected to the electric conductor.

ADVANTAGE - Improves electrostatic breakdown resistance. Reduces power supply noise since capacitance is connected between power supplies.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: LEAD FRAME PLASTIC PACKAGE TYPE IC LEAD THIN FILM INSULATE CONDUCTOR DEPOSIT CONNECT IC CHIP IMPROVE ELECTROSTATIC BREAKDOWN RESISTANCE

DERWENT-CLASS: U11

EPI-CODES: U11-D03A1A; U11-D03C1;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1995-056829

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平9－172059

(43)公開日　平成９年(1997)６月30日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０１Ｌ　21/68			Ｈ０１Ｌ　21/68	Ｕ	
Ｂ６５Ｄ　85/86		0333－3Ｅ	Ｂ６５Ｄ　85/38	Ｊ	

審査請求　未請求　請求項の数４　ＯＬ　（全　２　頁）

(21)出願番号　特願平7－328709

(22)出願日　平成７年(1995)12月18日

(71)出願人　390009667
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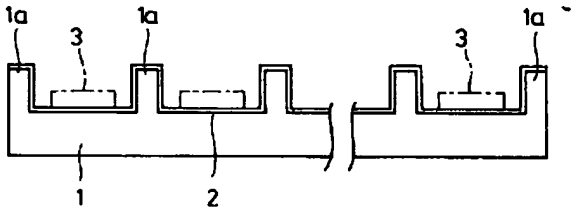
(72)発明者　鈴木　博己
栃木県那須郡塩原町大字下田野531－１
日本プレシジョン・サーキッツ株式会社内
(74)代理人　弁理士　松田　和子

(54)【発明の名称】　ＩＣ用チップトレイ

(57)【要約】
【課題】　ＩＣを静電気から確実に保護することが可能なＩＣ用チップトレイを提供する。
【解決手段】　ＩＣ用チップトレイの基体１の表面に金属層２をコーティングしてシート抵抗を大幅に減少させた。また、基体１の表面を凸凹状に形成して金属層２との密着性を向上させた。



DERWENT-ACC-NO: 1997-391235

DERWENT-WEEK: 199736

TITLE: Chip tray for IC - has base which surface is coated with metal layer thereby reducing sheet resistance of surface

PATENT-ASSIGNEE: NIPPON PRECISION CIRCUITS KK[NIPRN]

PRIORITY-DATA: 1995JP-0328709 (December 18, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 09172059 A	June 30, 1997	N/A	002	H01L 021/68

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 09172059A	N/A	1995JP-0328709	December 18, 1995

INT-CL (IPC): B65D085/86, H01L021/68

ABSTRACTED-PUB-NO: JP 09172059A

BASIC-ABSTRACT:

The chip tray has a base (1) which is coated with metal layer (2) thereby reducing sheet resistance of the surface.

The surface of the base is in the shape of unevenness.

ADVANTAGE - Performs guarding of IC from static.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: CHIP TRAY IC BASE SURFACE COATING METAL LAYER REDUCE SHEET RESISTANCE SURFACE

ADDL-INDEXING-TERMS:
ELECTROCONDUCTIVE PLASTICS

DERWENT-CLASS: Q34 U11

EPI-CODES: U11-F02A4;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1997-325694

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平11－181181

(43)公開日　平成11年(1999)７月６日

(51)Int.Cl.[6]	識別記号	ＦＩ
Ｃ０８Ｌ　23/10		Ｃ０８Ｌ　23/10
Ｃ０８Ｋ　3/00		Ｃ０８Ｋ　3/00
3/04		3/04
7/06		7/06
7/14		7/14

審査請求　未請求　請求項の数４　ＯＬ　（全 6 頁）　最終頁に続く

(21)出願番号　特願平9－356923

(22)出願日　平成９年(1997)12月25日

(71)出願人　000002141
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(72)発明者　中馬　敏秋
東京都品川区東品川２丁目５番８号　住友ベークライト株式会社内

(54)【発明の名称】　樹脂組成物

(57)【要約】
【課題】　射出成形などの成形加工性に良好であり、耐熱性、高機械強度、および帯電防止性に優れた樹脂組成物を提供すること。
【解決手段】　（ａ）ポリプロピレン樹脂１００重量部に対し、（ｂ）ガラス繊維４０～６０重量部（ｃ）無機フィラー３０～５０重量部（ｄ）カーボンブラック及び／又はカーボン繊維１０～９０重量部（ｅ）変性ポリプロピレン樹脂０．５～２０重量部を配合してなる樹脂組成物。

DERWENT-ACC-NO: 1999-439638

DERWENT-WEEK: 199941

TITLE: Resin composition with good mouldability - comprises polypropylene resin, glass fibre, inorganic fillers, carbon black and/or carbon fibre, and modified polypropylene resin

PATENT-ASSIGNEE: SUMITOMO BAKELITE CO LTD[SUMB]

PRIORITY-DATA: 1997JP-0356923 (December 25, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 11181181 A	July 6, 1999	N/A	006	C08L 023/10

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 11181181A	N/A	1997JP-0356923	December 25, 1997

INT-CL (IPC): C08K003/00, C08K003/04 , C08K007/06 , C08K007/14 , C08L023/10 , C08L023/10 , C08L023:26

ABSTRACTED-PUB-NO: JP 11181181A

BASIC-ABSTRACT:

Resin composition comprises (A) 100 pts. wt. of polypropylene resin with (B) 40-60 pts.wt. of glass fibre, (C) 30-50 pts. wt. of inorganic fillers, (D) 10-90 pts. wt.of carbon black and/or carbon fibre, and (E) 0.5-20 pts. wt. of modified polypropylene resin compounded.

USE - The resin compsn. is used as jigs for carrying electronic appts. and IC and packaging materials.

ADVANTAGE - The resin compsn. has good mouldability and antistatic properties and high thermal strength and mechanical strength.

CHOSEN-DRAWING: Dwg.0/0

TITLE-TERMS: RESIN COMPOSITION MOULD COMPRISE POLYPROPYLENE RESIN GLASS FIBRE INORGANIC FILL CARBON BLACK CARBON FIBRE MODIFIED POLYPROPYLENE RESIN

DERWENT-CLASS: A17 A85 A92 U11

CPI-CODES: A04-G03B; A07-A02; A08-R01;

EPI-CODES: U11-A07;

ENHANCED-POLYMER-INDEXING:
Polymer Index [1.1]
018 ; R00964 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D83 ; H0000 ; H0011*R ; P1150 ; P1343
Polymer Index [1.2]
018 ; G0044*R G0033 G0022 D01 D02 D12 D10 D51 D53 D58 ; R00964 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D83 ; H0011*R ; P1150
Polymer Index [1.3]
018 ; ND04 ; B9999 B3623 B3554 ; K9892 ; K9449 ; Q9999 Q7330*R ; Q9999 Q7476 Q7330 ; B9999 B4091*R B3838 B3747 ; B9999 B4148 B4091 B3838 B3747 ; B9999 B4159 B4091 B3838 B3747 ; B9999 B4171 B4091 B3838 B3747 ; B9999 B3601 B3554 ; B9999 B5594 B5572
Polymer Index [1.4]
018 ; G2891 D00 Si 4A ; A999 A419 ; S9999 S1070*R ; B9999 B5254 B5243 B4740
Polymer Index [1.5]
018 ; D00 G3190 R01541 F80 O* 6A Mg 2A Si 4A ; G3010 D00 F80 Al 3A Si 4A O* 6A ; A999 A237
Polymer Index [1.6]
018 ; R05085 D00 D09 C* 4A ; R05086 D00 D09 C* 4A ; A999 A602 A566 ; S9999 S1070*R
Polymer Index [1.7]
018 ; A999 A033
Polymer Index [2.1]
018 ; R00964 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D83 ; H0000 ; H0011*R ; M9999 M2391 ; M9999 M2062 ; A999 A782 ; A999 A033 ; P1150 ; P1343